

LOC	OBJECT CODE	ADDR1	ADDR2	STMT
				2 *****
				3 *
				4 *     Zvector E7 instruction tests for VRI-b instruction:
				5 *
				6 *     E746 VGM     - Vector Generate Mask
				7 *
				8 *             James Wekel April 2025
				9 *****
				11 *****
				12 *
				13 *             basic instruction tests
				14 *
				15 *****
				16 *     This program tests proper functioning of the z/arch E7 VRI-b
				17 *     Vector Generate Mask instruction.
				18 *     Exceptions are not tested.
				19 *
				20 *     PLEASE NOTE that the tests are very SIMPLE TESTS designed to catch
				21 *     obvious coding errors.   None of the tests are thorough.   They are
				22 *     NOT designed to test all aspects of any of the instructions.
				23 *
				24 *****
				25 *
				26 *     *Testcase zvector-e7-26-VGM
				27 *     *
				28 *     *     Zvector E7 instruction tests for VRI-b instruction:
				29 *     *
				30 *     *     E746 VGM     - Vector Generate Mask
				31 *     *
				32 *     *     # -----
				33 *     *     #     This tests only the basic function of the instruction.
				34 *     *     #     Exceptions are NOT tested.
				35 *     *     # -----
				36 *     *
				37 *     main size     2
				38 *     numcpu       1
				39 *     sysclear
				40 *     archlvl      z/Arch
				41 *     *
				42 *     loadcore     "\$(testpath)/zvector-e7-26-VGM core" 0x0
				43 *     *
				44 *     diag8cmd    enable     # (needed for messages to Hercules console)
				45 *     runtest     5
				46 *     diag8cmd    disable    # (reset back to default)
				47 *     *
				48 *     *Done
				49 *     *
				50 *****

LOC	OBJECT CODE	ADDR1	ADDR2	STMT
				52 *****
				53 * FCHECK Macro - Is a Facility Bit set?
				54 *
				55 * If the facility bit is NOT set, an message is issued and
				56 * the test is skipped.
				57 *
				58 * Fcheck uses R0, R1 and R2
				59 *
				60 * eg. FCHECK 134, 'vector-packed-decimal'
				61 *****
				62 MACRO
				63 FCHECK &BITNO, &NOTSETMSG
				64 . * &BITNO : facility bit number to check
				65 . * &NOTSETMSG : 'facility name'
				66 LCLA &FBBYTE Facility bit in Byte
				67 LCLA &FBBIT Facility bit within Byte
				68
				69 LCLA &L(8)
				70 &L(1) SetA 128, 64, 32, 16, 8, 4, 2, 1 bit positions within byte
				71
				72 &FBBYTE SETA &BITNO/8
				73 &FBBIT SETA &L((&BITNO-(&FBBYTE*8))+1)
				74 . * MNOTE 0, 'checking Bit=&BITNO: FBBYTE=&FBBYTE, FBBIT=&FBBIT'
				75
				76 B X&SYSNDX
				77 * Fcheck data area
				78 * skip messgae
				79 SKT&SYSNDX DC C' Skipping tests: '
				80 DC C&NOTSETMSG
				81 DC C' (bit &BITNO) is not installed.'
				82 SKL&SYSNDX EQU *-SKT&SYSNDX
				83 * facility bits
				84 DS FD gap
				85 FB&SYSNDX DS 4FD
				86 DS FD gap
				87 *
				88 X&SYSNDX EQU *
				89 LA R0, ((X&SYSNDX- FB&SYSNDX)/8)-1
				90 STFLE FB&SYSNDX get facility bits
				91
				92 XGR R0, R0
				93 IC R0, FB&SYSNDX+&FBBYTE get fbit byte
				94 N R0, =F' &FBBIT' is bit set?
				95 BNZ XC&SYSNDX
				96 *
				97 * facility bit not set, issue message and exit
				98 *
				99 LA R0, SKL&SYSNDX message length
				100 LA R1, SKT&SYSNDX message address
				101 BAL R2, MSG
				102
				103 B EOJ
				104 XC&SYSNDX EQU *
				105 MEND

LOC	OBJECT CODE	ADDR1	ADDR2	STMT	
				107	*****
				108	* Low core PSWs
				109	*****
00000000		00000000	00006A27	110	ZVE7TST START 0
		00000000		111	USING ZVE7TST, R0 Low core addressability
		00000140	00000000	112	
				113	SVOLDPSW EQU ZVE7TST+X' 140' z/Arch Supervisor call old PSW
00000000		00000000	000001A0	115	ORG ZVE7TST+X' 1A0' z/Architecture RESTART PSW
000001A0	00000001 80000000			116	DC X' 0000000180000000'
000001A8	00000000 00000200			117	DC AD(BEGIN)
000001B0		000001B0	000001D0	119	ORG ZVE7TST+X' 1D0' z/Architecture PROGRAM CHECK PSW
000001D0	00020001 80000000			120	DC X' 0002000180000000'
000001D8	00000000 0000DEAD			121	DC AD(X' DEAD')
000001E0		000001E0	00000200	123	ORG ZVE7TST+X' 200' Start of actual test program..
				125	*****
				126	* The actual "ZVE7TST" program itself...
				127	*****
				128	*
				129	* Architecture Mode: z/Arch
				130	* Register Usage:
				131	*
				132	* R0 (work)
				133	* R1- 4 (work)
				134	* R5 Testing control table - current test base
				135	* R6- R7 (work)
				136	* R8 First base register
				137	* R9 Second base register
				138	* R10 Third base register
				139	* R11 E7TEST call return
				140	* R12 E7TESTS register
				141	* R13 (work)
				142	* R14 Subroutine call
				143	* R15 Secondary Subroutine call or work
				144	*
				145	*****
00000200		00000200		147	USING BEGIN, R8 FIRST Base Register
00000200		00001200		148	USING BEGIN+4096, R9 SECOND Base Register
00000200		00002200		149	USING BEGIN+8192, R10 THIRD Base Register
00000200	0580			151	BEGIN BALR R8, 0 Inititalize FIRST base register
00000202	0680			152	BCTR R8, 0 Inititalize FIRST base register
00000204	0680			153	BCTR R8, 0 Inititalize FIRST base register
00000206	4190 8800		00000800	155	LA R9, 2048(, R8) Inititalize SECOND base register
0000020A	4190 9800		00000800	156	LA R9, 2048(, R9) Inititalize SECOND base register
				157	







LOC	OBJECT CODE			ADDR1	ADDR2	STMT				
						252	*****			
						253	*	RPTERROR	Report instruction test in error	
						254	*****			
00000326	50F0	81C0			000003C0	256	RPTERROR	ST	R15, RPTSAVE	Save return address
0000032A	5050	81C4			000003C4	257		ST	R5, RPTSVR5	Save R5
						258	*			
0000032E	4820	5004			00000004	259		LH	R2, TNUM	get test number and convert
00000332	4E20	8E8B			0000108B	260		CVD	R2, DECNUM	
00000336	D211	8E75	8E5F	00001075	0000105F	261		MVC	PRT3, EDIT	
0000033C	DE11	8E75	8E8B	00001075	0000108B	262		ED	PRT3, DECNUM	
00000342	D202	8E18	8E82	00001018	00001082	263		MVC	PRTNUM(3), PRT3+13	fill in message with test #
						264				
00000348	D207	8E33	500A	00001033	0000000A	265		MVC	PRTNAME, OPNAME	fill in message with instruction
						266	*			
0000034E	1722					267		XR	R2, R2	
00000350	4320	5008			00000008	268		IC	R2, I2	get i2 and convert
00000354	4E20	8E8B			0000108B	269		CVD	R2, DECNUM	
00000358	D211	8E75	8E5F	00001075	0000105F	270		MVC	PRT3, EDIT	
0000035E	DE11	8E75	8E8B	00001075	0000108B	271		ED	PRT3, DECNUM	
00000364	D201	8E44	8E83	00001044	00001083	272		MVC	PRTI2(2), PRT3+14	fill in message with i2 field
						273	*			
0000036A	1722					274		XR	R2, R2	
0000036C	4320	5009			00000009	275		IC	R2, I3	get i3 and convert
00000370	4E20	8E8B			0000108B	276		CVD	R2, DECNUM	
00000374	D211	8E75	8E5F	00001075	0000105F	277		MVC	PRT3, EDIT	
0000037A	DE11	8E75	8E8B	00001075	0000108B	278		ED	PRT3, DECNUM	
00000380	D201	8E50	8E83	00001050	00001083	279		MVC	PRTI3(2), PRT3+14	fill in message with i3 field
						280	*			
00000386	1722					281		XR	R2, R2	
00000388	4320	5007			00000007	282		IC	R2, M4	get M4 and convert
0000038C	4E20	8E8B			0000108B	283		CVD	R2, DECNUM	
00000390	D211	8E75	8E5F	00001075	0000105F	284		MVC	PRT3, EDIT	
00000396	DE11	8E75	8E8B	00001075	0000108B	285		ED	PRT3, DECNUM	
0000039C	D201	8E5C	8E83	0000105C	00001083	286		MVC	PRTM4(2), PRT3+14	fill in message with m4 field
						287	*			
						288	*			
						289	*			
000003A2	9002	81C8			000003C8	290		STM	R0, R2, RPTDWSAV	save regs used by MSG
000003A6	4100	0057			00000057	291		LA	R0, PRTLNG	message length
000003AA	4110	8E08			00001008	292		LA	R1, PRTLNE	messagfe address
000003AE	4520	81D8			000003D8	293		BAL	R2, MSG	call Hercules console MSG display
000003B2	9802	81C8			000003C8	294		LM	R0, R2, RPTDWSAV	restore regs
000003B6	5850	81C4			000003C4	296		L	R5, RPTSVR5	Restore R5
000003BA	58F0	81C0			000003C0	297		L	R15, RPTSAVE	Restore return address
000003BE	07FF					298		BR	R15	Return to caller
000003C0	00000000					300	RPTSAVE	DC	F' 0'	R15 save area
000003C4	00000000					301	RPTSVR5	DC	F' 0'	R5 save area
000003C8	00000000	00000000				303	RPTDWSAV	DC	2D' 0'	R0- R2 save area for MSG call













LOC	OBJECT CODE	ADDR1	ADDR2	STMT	
				425	*****
				426	*            E7TEST DSECT
				427	*****
				429	E7TEST    DSECT ,
00000000	00000000			430	TSUB       DC    A(0)            pointer to test
00000004	0000			431	TNUM       DC    H' 00'           Test Number
00000006	00			432	DC    X' 00'
				433	
00000007	00			434	M4          DC    HL1' 00'        M4 field
00000008	00			435	I2          DC    HL1' 00'        i2 used
00000009	00			436	I3          DC    Hl 1' 00'       i3 used
				437	
0000000A	40404040	40404040		438	OPNAME     DC    CL8' '           E7 name
00000014	00000000			439	V2ADDR     DC    A(0)           address of v2 source
00000018	00000000			440	V3ADDR     DC    A(0)           address of v3 source
0000001C	00000000			441	RELEN       DC    A(0)           RESULT LENGTH
00000020	00000000			442	READDR     DC    A(0)           result (expected) address
00000028	00000000	00000000		443	DS    FD            gap
00000030	00000000	00000000		444	V10OUTPUT   DS    XL16          V1 Output
00000040	00000000	00000000		445	DS    FD            gap
				446	
				447	*            test routine will be here (from VRI-b macro)
				448	*
				449	*            followed by
				450	*            EXPECTED RESULT
				452	ZVE7TST    CSECT ,
000010CC		00000000	00006A27	453	DS    0F
				455	*****
				456	*            Macros to help build test tables
				457	*****
				459	*
				460	*    macros to generate individual test
				461	*
				462	MACRO
				463	VRI_B &INST, &I2, &I3, &M4
				464	. *                                &INST    - VRI-b instruction under test
				465	. *                                &i2      - i2 field (unsigned decimal)
				466	. *                                &i3      - i3 field (unsigned decimal)
				467	. *                                &M4     - element size
				468	
				469	GBLA    &TNUM
				470	&TNUM       SETA    &TNUM+1
				471	
				472	DS    0FD
				473	USING *, R5            base for test data and test routine
				474	
				475	T&TNUM     DC    A(X&TNUM)       address of test routine

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
				476	DC	H' &TNUM	test number
				477	DC	X' 00'	
				478	DC	HL1' &M4'	M4 field
				479	DC	HL1' &I2'	i2 used
				480	DC	HL1' &I3'	i3 used
				481	DC	CL8' &INST'	instruction name
				482	DC	A(RE&TNUM+16)	address of v2 source
				483	DC	A(RE&TNUM+32)	address of v3 source
				484	DC	A(16)	result length
				485	REA&TNUM	DC A(RE&TNUM)	result address
				486	DS	FD	gap
				487	V10&TNUM	DS XL16	V1 output
				488	DS	FD	gap
				489	.	*	
				490	*		
				491	X&TNUM	DS 0F	
				492	VL	V22, V1FUDGE	
				493			
				494		&INST V22, &I2, &I3, &M4	test instruction (dest is a source)
				495			
				496	VST	V22, V10&TNUM	save v1 output
				497	BR	R11	return
				498			
				499	RE&TNUM	DC 0F	xl16 expected result
				500			
				501	DROP	R5	
				502	MEND		
				503	*		
				504	*	macro to generate table of pointers to individual tests	
				505	*		
				506		MACRO	
				507		PTTABLE	
				508		GBLA &TNUM	
				509		LCLA &CUR	
				510	&CUR	SETA 1	
				511	.	*	
				512	TTABLE	DS 0F	
				513	. LOOP	ANOP	
				514	.	*	
				515		DC A(T&CUR)	
				516	.	*	
				517	&CUR	SETA &CUR+1	
				518	AIF	(&CUR LE &TNUM) . LOOP	
				519	*		
				520	DC	A(0)	END OF TABLE
				521	DC	A(0)	
				522	.	*	
				523		MEND	
				524			

LOC	OBJECT CODE	ADDR1	ADDR2	STMT	
				526 *****	
				527 * E7 VRI-b tests	
				528 *****	
				529 PRINT DATA	
				530 *	
				531 * E746 VGM - Vector Generate Mask	
				532 *	
				533 * VRI_B instruction, I2, I3, M4	
				534 * followed by	
				535 * 16 byte expected result (V1)	
				536 *-----	
				537 * VGM - Vector Generate Mask	
				538 *-----	
				539 *Byte: I2<I3; I2=0	
				540 VRI_B VGM 0, 0, 0	
000010D0				541+ DS OFD	
000010D0		000010D0		542+ USING *, R5	base for test data and test routine
000010D0	00001118			543+T1 DC A(X1)	address of test routine
000010D4	0001			544+ DC H' 1'	test number
000010D6	00			545+ DC X' 00'	
000010D7	00			546+ DC HL1' 0'	M4 field
000010D8	00			547+ DC HL1' 0'	i2 used
000010D9	00			548+ DC HL1' 0'	i3 used
000010DA	E5C7D440 40404040			549+ DC CL8' VGM	instruction name
000010E4	0000113C			550+ DC A(RE1+16)	address of v2 source
000010E8	0000114C			551+ DC A(RE1+32)	address of v3 source
000010EC	00000010			552+ DC A(16)	result length
000010F0	0000112C			553+REA1 DC A(RE1)	result address
000010F8	00000000 00000000			554+ DS FD	gap
00001100	00000000 00000000			555+V101 DS XL16	V1 output
00001108	00000000 00000000				
00001110	00000000 00000000			556+ DS FD	gap
				557+*	
00001118				558+X1 DS OF	
00001118	E760 8EAC 0806	000010AC		559+ VL V22, V1FUDGE	
0000111E	E760 0000 0846			560+ VGM V22, 0, 0, 0	test instruction (dest is a source)
00001124	E760 5030 080E	00001100		561+ VST V22, V101	save v1 output
0000112A	07FB			562+ BR R11	return
0000112C				563+RE1 DC OF	xl16 expected result
0000112C				564+ DROP R5	
0000112C	80808080 80808080			565 DC XL16' 8080808080808080 8080808080808080'	result t
00001134	80808080 80808080				
				566	
				567 VRI_B VGM 0, 1, 0	
00001140				568+ DS OFD	
00001140		00001140		569+ USING *, R5	base for test data and test routine
00001140	00001188			570+T2 DC A(X2)	address of test routine
00001144	0002			571+ DC H' 2'	test number
00001146	00			572+ DC X' 00'	
00001147	00			573+ DC HL1' 0'	M4 field
00001148	00			574+ DC HL1' 0'	i2 used
00001149	01			575+ DC HL1' 1'	i3 used
0000114A	E5C7D440 40404040			576+ DC CL8' VGM	instruction name
00001154	000011AC			577+ DC A(RE2+16)	address of v2 source
00001158	000011BC			578+ DC A(RE2+32)	address of v3 source
0000115C	00000010			579+ DC A(16)	result length

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00001160	0000119C			580+REA2	DC	A(RE2)	result address
00001168	00000000 00000000			581+	DS	FD	gap
00001170	00000000 00000000			582+V102	DS	XL16	V1 output
00001178	00000000 00000000						
00001180	00000000 00000000			583+	DS	FD	gap
				584+*			
00001188				585+X2	DS	OF	
00001188	E760 8EAC 0806		000010AC	586+	VL	V22, V1FUDGE	
0000118E	E760 0001 0846			587+	VGM	V22, 0, 1, 0	test instruction (dest is a source)
00001194	E760 5030 080E		00001170	588+	VST	V22, V102	save v1 output
0000119A	07FB			589+	BR	R11	return
0000119C				590+REA2	DC	OF	xl16 expected result
0000119C				591+	DROP	R5	
0000119C	C0C0C0C0 C0C0C0C0			592	DC	XL16' C0C0C0C0C0C0C0C0 C0C0C0C0C0C0C0C0'	result
000011A4	C0C0C0C0 C0C0C0C0						
				593			
				594	VRI_B	VGM 0, 2, 0	
000011B0				595+	DS	OFD	
000011B0		000011B0		596+	USING	*, R5	base for test data and test routine
000011B0	000011F8			597+T3	DC	A(X3)	address of test routine
000011B4	0003			598+	DC	H' 3'	test number
000011B6	00			599+	DC	X' 00'	
000011B7	00			600+	DC	HL1' 0'	M4 field
000011B8	00			601+	DC	HL1' 0'	i2 used
000011B9	02			602+	DC	HL1' 2'	i3 used
000011BA	E5C7D440 40404040			603+	DC	CL8' VGM	instruction name
000011C4	0000121C			604+	DC	A(RE3+16)	address of v2 source
000011C8	0000122C			605+	DC	A(RE3+32)	address of v3 source
000011CC	00000010			606+	DC	A(16)	result length
000011D0	0000120C			607+REA3	DC	A(RE3)	result address
000011D8	00000000 00000000			608+	DS	FD	gap
000011E0	00000000 00000000			609+V103	DS	XL16	V1 output
000011E8	00000000 00000000						
000011F0	00000000 00000000			610+	DS	FD	gap
				611+*			
000011F8				612+X3	DS	OF	
000011F8	E760 8EAC 0806		000010AC	613+	VL	V22, V1FUDGE	
000011FE	E760 0002 0846			614+	VGM	V22, 0, 2, 0	test instruction (dest is a source)
00001204	E760 5030 080E		000011E0	615+	VST	V22, V103	save v1 output
0000120A	07FB			616+	BR	R11	return
0000120C				617+RE3	DC	OF	xl16 expected result
0000120C				618+	DROP	R5	
0000120C	E0E0E0E0 E0E0E0E0			619	DC	XL16' E0E0E0E0E0E0E0E0 E0E0E0E0E0E0E0E0'	result
00001214	E0E0E0E0 E0E0E0E0						
				620			
				621	VRI_B	VGM 0, 4, 0	
00001220				622+	DS	OFD	
00001220		00001220		623+	USING	*, R5	base for test data and test routine
00001220	00001268			624+T4	DC	A(X4)	address of test routine
00001224	0004			625+	DC	H' 4'	test number
00001226	00			626+	DC	X' 00'	
00001227	00			627+	DC	HL1' 0'	M4 field
00001228	00			628+	DC	HL1' 0'	i2 used
00001229	04			629+	DC	HL1' 4'	i3 used
0000122A	E5C7D440 40404040			630+	DC	CL8' VGM	instruction name
00001234	0000128C			631+	DC	A(RE4+16)	address of v2 source



LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00001238	0000129C			632+	DC	A(RE4+32)	address of v3 source
0000123C	00000010			633+	DC	A(16)	result length
00001240	0000127C			634+REA4	DC	A(RE4)	result address
00001248	00000000 00000000			635+	DS	FD	gap
00001250	00000000 00000000			636+V104	DS	XL16	V1 output
00001258	00000000 00000000						
00001260	00000000 00000000			637+	DS	FD	gap
				638+*			
00001268				639+X4	DS	0F	
00001268	E760 8EAC 0806		000010AC	640+	VL	V22, V1FUDGE	
0000126E	E760 0004 0846			641+	VGM	V22, 0, 4, 0	test instruction (dest is a source)
00001274	E760 5030 080E		00001250	642+	VST	V22, V104	save v1 output
0000127A	07FB			643+	BR	R11	return
0000127C				644+RE4	DC	0F	xl16 expected result
0000127C				645+	DROP	R5	
0000127C	F8F8F8F8 F8F8F8F8			646	DC	XL16' F8F8F8F8F8F8F8F8 F8F8F8F8F8F8F8F8'	result t
00001284	F8F8F8F8 F8F8F8F8						
				647			
				648	VRI_B	VGM 0, 6, 0	
00001290				649+	DS	0FD	
00001290		00001290		650+	USING	*, R5	base for test data and test routine
00001290	000012D8			651+T5	DC	A(X5)	address of test routine
00001294	0005			652+	DC	H' 5'	test number
00001296	00			653+	DC	X' 00'	
00001297	00			654+	DC	HL1' 0'	M4 field
00001298	00			655+	DC	HL1' 0'	i2 used
00001299	06			656+	DC	HL1' 6'	i3 used
0000129A	E5C7D440 40404040			657+	DC	CL8' VGM	instruction name
000012A4	000012FC			658+	DC	A(RE5+16)	address of v2 source
000012A8	0000130C			659+	DC	A(RE5+32)	address of v3 source
000012AC	00000010			660+	DC	A(16)	result length
000012B0	000012EC			661+REA5	DC	A(RE5)	result address
000012B8	00000000 00000000			662+	DS	FD	gap
000012C0	00000000 00000000			663+V105	DS	XL16	V1 output
000012C8	00000000 00000000						
000012D0	00000000 00000000			664+	DS	FD	gap
				665+*			
000012D8				666+X5	DS	0F	
000012D8	E760 8EAC 0806		000010AC	667+	VL	V22, V1FUDGE	
000012DE	E760 0006 0846			668+	VGM	V22, 0, 6, 0	test instruction (dest is a source)
000012E4	E760 5030 080E		000012C0	669+	VST	V22, V105	save v1 output
000012EA	07FB			670+	BR	R11	return
000012EC				671+RE5	DC	0F	xl16 expected result
000012EC				672+	DROP	R5	
000012EC	FEFEFEFE FEFEFEFE			673	DC	XL16' FEFEFEFEFEFEFEFEFE FEFEFEFEFEFEFEFE'	result t
000012F4	FEFEFEFE FEFEFEFE						
				674			
				675	VRI_B	VGM 0, 7, 0	
00001300				676+	DS	0FD	
00001300		00001300		677+	USING	*, R5	base for test data and test routine
00001300	00001348			678+T6	DC	A(X6)	address of test routine
00001304	0006			679+	DC	H' 6'	test number
00001306	00			680+	DC	X' 00'	
00001307	00			681+	DC	HL1' 0'	M4 field
00001308	00			682+	DC	HL1' 0'	i2 used
00001309	07			683+	DC	HL1' 7'	i3 used



LOC	OBJECT CODE	ADDR1	ADDR2	STMT	
				704 *Byte: I2<I3; I2=1	
				705 VRI_B VGM 1, 1, 0	
00001370				706+ DS OFD	
00001370		00001370		707+ USING *, R5	base for test data and test routine
00001370	000013B8			708+T7 DC A(X7)	address of test routine
00001374	0007			709+ DC H' 7'	test number
00001376	00			710+ DC X' 00'	
00001377	00			711+ DC HL1' 0'	M4 field
00001378	01			712+ DC HL1' 1'	i2 used
00001379	01			713+ DC HL1' 1'	i3 used
0000137A	E5C7D440 40404040			714+ DC CL8' VGM	instruction name
00001384	000013DC			715+ DC A(RE7+16)	address of v2 source
00001388	000013EC			716+ DC A(RE7+32)	address of v3 source
0000138C	00000010			717+ DC A(16)	result length
00001390	000013CC			718+REA7 DC A(RE7)	result address
00001398	00000000 00000000			719+ DS FD	gap
000013A0	00000000 00000000			720+V107 DS XL16	V1 output
000013A8	00000000 00000000				
000013B0	00000000 00000000			721+ DS FD	gap
				722+*	
000013B8				723+X7 DS OF	
000013B8	E760 8EAC 0806		000010AC	724+ VL V22, V1FUDGE	
000013BE	E760 0101 0846			725+ VGM V22, 1, 1, 0	test instruction (dest is a source)
000013C4	E760 5030 080E		000013A0	726+ VST V22, V107	save v1 output
000013CA	07FB			727+ BR R11	return
000013CC				728+RE7 DC OF	xl16 expected result
000013CC				729+ DROP R5	
000013CC	40404040 40404040			730 DC XL16' 4040404040404040 4040404040404040'	result t
000013D4	40404040 40404040				
				731	
				732 VRI_B VGM 1, 2, 0	
000013E0				733+ DS OFD	
000013E0		000013E0		734+ USING *, R5	base for test data and test routine
000013E0	00001428			735+T8 DC A(X8)	address of test routine
000013E4	0008			736+ DC H' 8'	test number
000013E6	00			737+ DC X' 00'	
000013E7	00			738+ DC HL1' 0'	M4 field
000013E8	01			739+ DC HL1' 1'	i2 used
000013E9	02			740+ DC HL1' 2'	i3 used
000013EA	E5C7D440 40404040			741+ DC CL8' VGM	instruction name
000013F4	0000144C			742+ DC A(RE8+16)	address of v2 source
000013F8	0000145C			743+ DC A(RE8+32)	address of v3 source
000013FC	00000010			744+ DC A(16)	result length
00001400	0000143C			745+REA8 DC A(RE8)	result address
00001408	00000000 00000000			746+ DS FD	gap
00001410	00000000 00000000			747+V108 DS XL16	V1 output
00001418	00000000 00000000				
00001420	00000000 00000000			748+ DS FD	gap
				749+*	
00001428				750+X8 DS OF	
00001428	E760 8EAC 0806		000010AC	751+ VL V22, V1FUDGE	
0000142E	E760 0102 0846			752+ VGM V22, 1, 2, 0	test instruction (dest is a source)
00001434	E760 5030 080E		00001410	753+ VST V22, V108	save v1 output
0000143A	07FB			754+ BR R11	return
0000143C				755+RE8 DC OF	xl16 expected result
0000143C				756+ DROP R5	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
0000143C	60606060 60606060			757	DC	XL16' 6060606060606060 6060606060606060'	result
00001444	60606060 60606060						
				758			
				759	VRI_B	VGM 1, 4, 0	
00001450				760+	DS	OFD	
00001450		00001450		761+	USING	*, R5	base for test data and test routine
00001450	00001498			762+T9	DC	A(X9)	address of test routine
00001454	0009			763+	DC	H' 9'	test number
00001456	00			764+	DC	X' 00'	
00001457	00			765+	DC	HL1' 0'	M4 field
00001458	01			766+	DC	HL1' 1'	i2 used
00001459	04			767+	DC	HL1' 4'	i3 used
0000145A	E5C7D440 40404040			768+	DC	CL8' VGM	instruction name
00001464	000014BC			769+	DC	A(RE9+16)	address of v2 source
00001468	000014CC			770+	DC	A(RE9+32)	address of v3 source
0000146C	00000010			771+	DC	A(16)	result length
00001470	000014AC			772+REA9	DC	A(RE9)	result address
00001478	00000000 00000000			773+	DS	FD	gap
00001480	00000000 00000000			774+V109	DS	XL16	V1 output
00001488	00000000 00000000						
00001490	00000000 00000000			775+	DS	FD	gap
				776+*			
00001498				777+X9	DS	OF	
00001498	E760 8EAC 0806		000010AC	778+	VL	V22, V1FUDGE	
0000149E	E760 0104 0846			779+	VGM	V22, 1, 4, 0	test instruction (dest is a source)
000014A4	E760 5030 080E		00001480	780+	VST	V22, V109	save v1 output
000014AA	07FB			781+	BR	R11	return
000014AC				782+RE9	DC	OF	xl16 expected result
000014AC				783+	DROP	R5	
000014AC	78787878 78787878			784	DC	XL16' 7878787878787878 7878787878787878'	result
000014B4	78787878 78787878						
				785			
				786	VRI_B	VGM 1, 6, 0	
000014C0				787+	DS	OFD	
000014C0		000014C0		788+	USING	*, R5	base for test data and test routine
000014C0	00001508			789+T10	DC	A(X10)	address of test routine
000014C4	000A			790+	DC	H' 10'	test number
000014C6	00			791+	DC	X' 00'	
000014C7	00			792+	DC	HL1' 0'	M4 field
000014C8	01			793+	DC	HL1' 1'	i2 used
000014C9	06			794+	DC	HL1' 6'	i3 used
000014CA	E5C7D440 40404040			795+	DC	CL8' VGM	instruction name
000014D4	0000152C			796+	DC	A(RE10+16)	address of v2 source
000014D8	0000153C			797+	DC	A(RE10+32)	address of v3 source
000014DC	00000010			798+	DC	A(16)	result length
000014E0	0000151C			799+REA10	DC	A(RE10)	result address
000014E8	00000000 00000000			800+	DS	FD	gap
000014F0	00000000 00000000			801+V1010	DS	XL16	V1 output
000014F8	00000000 00000000						
00001500	00000000 00000000			802+	DS	FD	gap
				803+*			
00001508				804+X10	DS	OF	
00001508	E760 8EAC 0806		000010AC	805+	VL	V22, V1FUDGE	
0000150E	E760 0106 0846			806+	VGM	V22, 1, 6, 0	test instruction (dest is a source)
00001514	E760 5030 080E		000014F0	807+	VST	V22, V1010	save v1 output
0000151A	07FB			808+	BR	R11	return





LOC	OBJECT CODE	ADDR1	ADDR2	STMT	
				842 *Byte: I2>I3; I3=0	
				843 VRI_B VGM 1, 0, 0	
000015A0				844+ DS OFD	
000015A0		000015A0		845+ USING *, R5	base for test data and test routine
000015A0	000015E8			846+T12 DC A(X12)	address of test routine
000015A4	000C			847+ DC H' 12'	test number
000015A6	00			848+ DC X' 00'	
000015A7	00			849+ DC HL1' 0'	M4 field
000015A8	01			850+ DC HL1' 1'	i2 used
000015A9	00			851+ DC HL1' 0'	i3 used
000015AA	E5C7D440 40404040			852+ DC CL8' VGM	instruction name
000015B4	0000160C			853+ DC A(RE12+16)	address of v2 source
000015B8	0000161C			854+ DC A(RE12+32)	address of v3 source
000015BC	00000010			855+ DC A(16)	result length
000015C0	000015FC			856+REA12 DC A(RE12)	result address
000015C8	00000000 00000000			857+ DS FD	gap
000015D0	00000000 00000000			858+V1012 DS XL16	V1 output
000015D8	00000000 00000000				
000015E0	00000000 00000000			859+ DS FD	gap
				860+*	
000015E8				861+X12 DS OF	
000015E8	E760 8EAC 0806		000010AC	862+ VL V22, V1FUDGE	
000015EE	E760 0100 0846			863+ VGM V22, 1, 0, 0	test instruction (dest is a source)
000015F4	E760 5030 080E		000015D0	864+ VST V22, V1012	save v1 output
000015FA	07FB			865+ BR R11	return
000015FC				866+RE12 DC OF	xl16 expected result
000015FC				867+ DROP R5	
000015FC	FFFFFFFF FFFFFFFF			868 DC XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF'	result t
00001604	FFFFFFFF FFFFFFFF				
				869	
				870 VRI_B VGM 2, 0, 0	
00001610				871+ DS OFD	
00001610		00001610		872+ USING *, R5	base for test data and test routine
00001610	00001658			873+T13 DC A(X13)	address of test routine
00001614	000D			874+ DC H' 13'	test number
00001616	00			875+ DC X' 00'	
00001617	00			876+ DC HL1' 0'	M4 field
00001618	02			877+ DC HL1' 2'	i2 used
00001619	00			878+ DC HL1' 0'	i3 used
0000161A	E5C7D440 40404040			879+ DC CL8' VGM	instruction name
00001624	0000167C			880+ DC A(RE13+16)	address of v2 source
00001628	0000168C			881+ DC A(RE13+32)	address of v3 source
0000162C	00000010			882+ DC A(16)	result length
00001630	0000166C			883+REA13 DC A(RE13)	result address
00001638	00000000 00000000			884+ DS FD	gap
00001640	00000000 00000000			885+V1013 DS XL16	V1 output
00001648	00000000 00000000				
00001650	00000000 00000000			886+ DS FD	gap
				887+*	
00001658				888+X13 DS OF	
00001658	E760 8EAC 0806		000010AC	889+ VL V22, V1FUDGE	
0000165E	E760 0200 0846			890+ VGM V22, 2, 0, 0	test instruction (dest is a source)
00001664	E760 5030 080E		00001640	891+ VST V22, V1013	save v1 output
0000166A	07FB			892+ BR R11	return
0000166C				893+RE13 DC OF	xl16 expected result
0000166C				894+ DROP R5	







LOC	OBJECT CODE	ADDR1	ADDR2	STMT	
				980 *Byte: I2>I3; I3=1	
				981 VRI_B VGM 2, 1, 0	
000017D0				982+ DS OFD	
000017D0		000017D0		983+ USING *, R5	base for test data and test routine
000017D0	00001818			984+T17 DC A(X17)	address of test routine
000017D4	0011			985+ DC H' 17'	test number
000017D6	00			986+ DC X' 00'	
000017D7	00			987+ DC HL1' 0'	M4 field
000017D8	02			988+ DC HL1' 2'	i2 used
000017D9	01			989+ DC HL1' 1'	i3 used
000017DA	E5C7D440 40404040			990+ DC CL8' VGM	instruction name
000017E4	0000183C			991+ DC A(RE17+16)	address of v2 source
000017E8	0000184C			992+ DC A(RE17+32)	address of v3 source
000017EC	00000010			993+ DC A(16)	result length
000017F0	0000182C			994+REA17 DC A(RE17)	result address
000017F8	00000000 00000000			995+ DS FD	gap
00001800	00000000 00000000			996+V1017 DS XL16	V1 output
00001808	00000000 00000000				
00001810	00000000 00000000			997+ DS FD	gap
				998+*	
00001818				999+X17 DS OF	
00001818	E760 8EAC 0806		000010AC	1000+ VL V22, V1FUDGE	
0000181E	E760 0201 0846			1001+ VGM V22, 2, 1, 0	test instruction (dest is a source)
00001824	E760 5030 080E		00001800	1002+ VST V22, V1017	save v1 output
0000182A	07FB			1003+ BR R11	return
0000182C				1004+RE17 DC OF	xl16 expected result
0000182C				1005+ DROP R5	
0000182C	FFFFFFFF FFFFFFFF			1006 DC XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF'	result t
00001834	FFFFFFFF FFFFFFFF				
				1007	
				1008 VRI_B VGM 4, 1, 0	
00001840				1009+ DS OFD	
00001840		00001840		1010+ USING *, R5	base for test data and test routine
00001840	00001888			1011+T18 DC A(X18)	address of test routine
00001844	0012			1012+ DC H' 18'	test number
00001846	00			1013+ DC X' 00'	
00001847	00			1014+ DC HL1' 0'	M4 field
00001848	04			1015+ DC HL1' 4'	i2 used
00001849	01			1016+ DC HL1' 1'	i3 used
0000184A	E5C7D440 40404040			1017+ DC CL8' VGM	instruction name
00001854	000018AC			1018+ DC A(RE18+16)	address of v2 source
00001858	000018BC			1019+ DC A(RE18+32)	address of v3 source
0000185C	00000010			1020+ DC A(16)	result length
00001860	0000189C			1021+REA18 DC A(RE18)	result address
00001868	00000000 00000000			1022+ DS FD	gap
00001870	00000000 00000000			1023+V1018 DS XL16	V1 output
00001878	00000000 00000000				
00001880	00000000 00000000			1024+ DS FD	gap
				1025+*	
00001888				1026+X18 DS OF	
00001888	E760 8EAC 0806		000010AC	1027+ VL V22, V1FUDGE	
0000188E	E760 0401 0846			1028+ VGM V22, 4, 1, 0	test instruction (dest is a source)
00001894	E760 5030 080E		00001870	1029+ VST V22, V1018	save v1 output
0000189A	07FB			1030+ BR R11	return
0000189C				1031+RE18 DC OF	xl16 expected result
0000189C				1032+ DROP R5	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT		
0000189C	CFCFCFCF CFCFCFCF			1033	DC	XL16' CFCFCFCFCFCFCFCF CFCFCFCFCFCFCFCF' result t
000018A4	CFCFCFCF CFCFCFCF					
				1034		
000018B0				1035	VRI_B	VGM 6, 1, 0
000018B0		000018B0		1036+	DS	OFD
000018B0	000018F8			1037+	USING	*, R5
000018B4	0013			1038+T19	DC	A(X19)
000018B6	00			1039+	DC	H' 19'
000018B7	00			1040+	DC	X' 00'
000018B8	06			1041+	DC	HL1' 0'
000018B9	01			1042+	DC	HL1' 6'
000018BA	E5C7D440 40404040			1043+	DC	HL1' 1'
000018C4	0000191C			1044+	DC	CL8' VGM
000018C8	0000192C			1045+	DC	A(RE19+16)
000018CC	00000010			1046+	DC	A(RE19+32)
000018D0	0000190C			1047+	DC	A(16)
000018D8	00000000 00000000			1048+REA19	DC	A(RE19)
000018E0	00000000 00000000			1049+	DS	FD
000018E8	00000000 00000000			1050+V1019	DS	XL16
000018F0	00000000 00000000					
				1051+	DS	FD
000018F8				1052+*		gap
000018F8	E760 8EAC 0806		000010AC	1053+X19	DS	OF
000018FE	E760 0601 0846			1054+	VL	V22, V1FUDGE
00001904	E760 5030 080E		000018E0	1055+	VGM	V22, 6, 1, 0
0000190A	07FB			1056+	VST	V22, V1019
0000190C				1057+	BR	R11
0000190C				1058+RE19	DC	OF
0000190C				1059+	DROP	R5
0000190C	C3C3C3C3 C3C3C3C3			1060	DC	XL16' C3C3C3C3C3C3C3C3 C3C3C3C3C3C3C3C3' result t
00001914	C3C3C3C3 C3C3C3C3					
				1061		
00001920				1062	VRI_B	VGM 7, 1, 0
00001920		00001920		1063+	DS	OFD
00001920	00001968			1064+	USING	*, R5
00001924	0014			1065+T20	DC	A(X20)
00001926	00			1066+	DC	H' 20'
00001927	00			1067+	DC	X' 00'
00001928	07			1068+	DC	HL1' 0'
00001929	01			1069+	DC	HL1' 7'
0000192A	E5C7D440 40404040			1070+	DC	HL1' 1'
00001934	0000198C			1071+	DC	CL8' VGM
00001938	0000199C			1072+	DC	A(RE20+16)
0000193C	00000010			1073+	DC	A(RE20+32)
00001940	0000197C			1074+	DC	A(16)
00001948	00000000 00000000			1075+REA20	DC	A(RE20)
00001950	00000000 00000000			1076+	DS	FD
00001958	00000000 00000000			1077+V1020	DS	XL16
00001960	00000000 00000000					
				1078+	DS	FD
00001968				1079+*		gap
00001968	E760 8EAC 0806		000010AC	1080+X20	DS	OF
0000196E	E760 0701 0846			1081+	VL	V22, V1FUDGE
00001974	E760 5030 080E		00001950	1082+	VGM	V22, 7, 1, 0
0000197A	07FB			1083+	VST	V22, V1020
				1084+	BR	R11



LOC	OBJECT CODE	ADDR1	ADDR2	STMT	
				1118 *Halfword: I2<I3; I2=0	
				1119 VRI_B VGM 0, 0, 1	
00001A00				1120+ DS OFD	
00001A00		00001A00		1121+ USING *, R5	base for test data and test routine
00001A00	00001A48			1122+T22 DC A(X22)	address of test routine
00001A04	0016			1123+ DC H' 22'	test number
00001A06	00			1124+ DC X' 00'	
00001A07	01			1125+ DC HL1' 1'	M4 field
00001A08	00			1126+ DC HL1' 0'	i2 used
00001A09	00			1127+ DC HL1' 0'	i3 used
00001A0A	E5C7D440 40404040			1128+ DC CL8' VGM	instruction name
00001A14	00001A6C			1129+ DC A(RE22+16)	address of v2 source
00001A18	00001A7C			1130+ DC A(RE22+32)	address of v3 source
00001A1C	00000010			1131+ DC A(16)	result length
00001A20	00001A5C			1132+REA22 DC A(RE22)	result address
00001A28	00000000 00000000			1133+ DS FD	gap
00001A30	00000000 00000000			1134+V1022 DS XL16	V1 output
00001A38	00000000 00000000				
00001A40	00000000 00000000			1135+ DS FD	gap
				1136+*	
00001A48				1137+X22 DS OF	
00001A48	E760 8EAC 0806		000010AC	1138+ VL V22, V1FUDGE	
00001A4E	E760 0000 1846			1139+ VGM V22, 0, 0, 1	test instruction (dest is a source)
00001A54	E760 5030 080E		00001A30	1140+ VST V22, V1022	save v1 output
00001A5A	07FB			1141+ BR R11	return
00001A5C				1142+RE22 DC OF	xl16 expected result
00001A5C				1143+ DROP R5	
00001A5C	80008000 80008000			1144 DC XL16' 8000800080008000 8000800080008000'	result
00001A64	80008000 80008000				
				1145	
				1146 VRI_B VGM 0, 1, 1	
00001A70				1147+ DS OFD	
00001A70		00001A70		1148+ USING *, R5	base for test data and test routine
00001A70	00001AB8			1149+T23 DC A(X23)	address of test routine
00001A74	0017			1150+ DC H' 23'	test number
00001A76	00			1151+ DC X' 00'	
00001A77	01			1152+ DC HL1' 1'	M4 field
00001A78	00			1153+ DC HL1' 0'	i2 used
00001A79	01			1154+ DC HL1' 1'	i3 used
00001A7A	E5C7D440 40404040			1155+ DC CL8' VGM	instruction name
00001A84	00001ADC			1156+ DC A(RE23+16)	address of v2 source
00001A88	00001AEC			1157+ DC A(RE23+32)	address of v3 source
00001A8C	00000010			1158+ DC A(16)	result length
00001A90	00001ACC			1159+REA23 DC A(RE23)	result address
00001A98	00000000 00000000			1160+ DS FD	gap
00001AA0	00000000 00000000			1161+V1023 DS XL16	V1 output
00001AA8	00000000 00000000				
00001AB0	00000000 00000000			1162+ DS FD	gap
				1163+*	
00001AB8				1164+X23 DS OF	
00001AB8	E760 8EAC 0806		000010AC	1165+ VL V22, V1FUDGE	
00001ABE	E760 0001 1846			1166+ VGM V22, 0, 1, 1	test instruction (dest is a source)
00001AC4	E760 5030 080E		00001AA0	1167+ VST V22, V1023	save v1 output
00001ACA	07FB			1168+ BR R11	return
00001ACC				1169+RE23 DC OF	xl16 expected result
00001ACC				1170+ DROP R5	



LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00001ACC 00001AD4	C000C000 C000C000 C000C000 C000C000			1171	DC	XL16' C000C000C000C000 C000C000C000C000'	result
				1172			
00001AE0				1173	VRI_B	VGM 0, 2, 1	
00001AE0		00001AE0		1174+	DS	OFD	
00001AE0	00001B28			1175+	USING	*, R5	base for test data and test routine
00001AE4	0018			1176+T24	DC	A(X24)	address of test routine
00001AE6	00			1177+	DC	H' 24'	test number
00001AE7	01			1178+	DC	X' 00'	
00001AE8	00			1179+	DC	HL1' 1'	M4 field
00001AE9	02			1180+	DC	HL1' 0'	i2 used
00001AEA	E5C7D440 40404040			1181+	DC	HL1' 2'	i3 used
00001AF4	00001B4C			1182+	DC	CL8' VGM	instruction name
00001AF8	00001B5C			1183+	DC	A(RE24+16)	address of v2 source
00001AFC	00000010			1184+	DC	A(RE24+32)	address of v3 source
00001B00	00001B3C			1185+	DC	A(16)	result length
00001B08	00000000 00000000			1186+REA24	DC	A(RE24)	result address
00001B10	00000000 00000000			1187+	DS	FD	gap
00001B18	00000000 00000000			1188+V1024	DS	XL16	V1 output
00001B20	00000000 00000000			1189+	DS	FD	gap
				1190+*			
00001B28				1191+X24	DS	OF	
00001B28	E760 8EAC 0806		000010AC	1192+	VL	V22, V1FUDGE	
00001B2E	E760 0002 1846			1193+	VGM	V22, 0, 2, 1	test instruction (dest is a source)
00001B34	E760 5030 080E		00001B10	1194+	VST	V22, V1024	save v1 output
00001B3A	07FB			1195+	BR	R11	return
00001B3C				1196+RE24	DC	OF	xl16 expected result
00001B3C	E000E000 E000E000			1197+	DROP	R5	
00001B44	E000E000 E000E000			1198	DC	XL16' E000E000E000E000 E000E000E000E000'	result
				1199			
00001B50				1200	VRI_B	VGM 0, 4, 1	
00001B50		00001B50		1201+	DS	OFD	
00001B50	00001B98			1202+	USING	*, R5	base for test data and test routine
00001B54	0019			1203+T25	DC	A(X25)	address of test routine
00001B56	00			1204+	DC	H' 25'	test number
00001B57	01			1205+	DC	X' 00'	
00001B58	00			1206+	DC	HL1' 1'	M4 field
00001B59	04			1207+	DC	HL1' 0'	i2 used
00001B5A	E5C7D440 40404040			1208+	DC	HL1' 4'	i3 used
00001B64	00001BBC			1209+	DC	CL8' VGM	instruction name
00001B68	00001BCC			1210+	DC	A(RE25+16)	address of v2 source
00001B6C	00000010			1211+	DC	A(RE25+32)	address of v3 source
00001B70	00001BAC			1212+	DC	A(16)	result length
00001B78	00000000 00000000			1213+REA25	DC	A(RE25)	result address
00001B80	00000000 00000000			1214+	DS	FD	gap
00001B88	00000000 00000000			1215+V1025	DS	XL16	V1 output
00001B90	00000000 00000000			1216+	DS	FD	gap
				1217+*			
00001B98				1218+X25	DS	OF	
00001B98	E760 8EAC 0806		000010AC	1219+	VL	V22, V1FUDGE	
00001B9E	E760 0004 1846			1220+	VGM	V22, 0, 4, 1	test instruction (dest is a source)
00001BA4	E760 5030 080E		00001B80	1221+	VST	V22, V1025	save v1 output
00001BAA	07FB			1222+	BR	R11	return

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00001BAC				1223+RE25	DC	0F	xl16 expected result
00001BAC				1224+	DROP	R5	
00001BAC	F800F800 F800F800			1225	DC	XL16' F800F800F800F800 F800F800F800F800'	result
00001BB4	F800F800 F800F800						
				1226			
				1227	VRI_B	VGM 0, 6, 1	
00001BC0				1228+	DS	0FD	
00001BC0		00001BC0		1229+	USING	*, R5	base for test data and test routine
00001BC0	00001C08			1230+T26	DC	A(X26)	address of test routine
00001BC4	001A			1231+	DC	H' 26'	test number
00001BC6	00			1232+	DC	X' 00'	
00001BC7	01			1233+	DC	HL1' 1'	M4 field
00001BC8	00			1234+	DC	HL1' 0'	i2 used
00001BC9	06			1235+	DC	HL1' 6'	i3 used
00001BCA	E5C7D440 40404040			1236+	DC	CL8' VGM	instruction name
00001BD4	00001C2C			1237+	DC	A(RE26+16)	address of v2 source
00001BD8	00001C3C			1238+	DC	A(RE26+32)	address of v3 source
00001BDC	00000010			1239+	DC	A(16)	result length
00001BE0	00001C1C			1240+REA26	DC	A(RE26)	result address
00001BE8	00000000 00000000			1241+	DS	FD	gap
00001BF0	00000000 00000000			1242+V1026	DS	XL16	V1 output
00001BF8	00000000 00000000						
00001C00	00000000 00000000			1243+	DS	FD	gap
				1244+*			
00001C08				1245+X26	DS	0F	
00001C08	E760 8EAC 0806		000010AC	1246+	VL	V22, V1FUDGE	
00001C0E	E760 0006 1846			1247+	VGM	V22, 0, 6, 1	test instruction (dest is a source)
00001C14	E760 5030 080E		00001BF0	1248+	VST	V22, V1026	save v1 output
00001C1A	07FB			1249+	BR	R11	return
00001C1C				1250+RE26	DC	0F	xl16 expected result
00001C1C				1251+	DROP	R5	
00001C1C	FE00FE00 FE00FE00			1252	DC	XL16' FE00FE00FE00FE00 FE00FE00FE00FE00'	result
00001C24	FE00FE00 FE00FE00						
				1253			
				1254	VRI_B	VGM 0, 7, 1	
00001C30				1255+	DS	0FD	
00001C30		00001C30		1256+	USING	*, R5	base for test data and test routine
00001C30	00001C78			1257+T27	DC	A(X27)	address of test routine
00001C34	001B			1258+	DC	H' 27'	test number
00001C36	00			1259+	DC	X' 00'	
00001C37	01			1260+	DC	HL1' 1'	M4 field
00001C38	00			1261+	DC	HL1' 0'	i2 used
00001C39	07			1262+	DC	HL1' 7'	i3 used
00001C3A	E5C7D440 40404040			1263+	DC	CL8' VGM	instruction name
00001C44	00001C9C			1264+	DC	A(RE27+16)	address of v2 source
00001C48	00001CAC			1265+	DC	A(RE27+32)	address of v3 source
00001C4C	00000010			1266+	DC	A(16)	result length
00001C50	00001C8C			1267+REA27	DC	A(RE27)	result address
00001C58	00000000 00000000			1268+	DS	FD	gap
00001C60	00000000 00000000			1269+V1027	DS	XL16	V1 output
00001C68	00000000 00000000						
00001C70	00000000 00000000			1270+	DS	FD	gap
				1271+*			
00001C78				1272+X27	DS	0F	
00001C78	E760 8EAC 0806		000010AC	1273+	VL	V22, V1FUDGE	
00001C7E	E760 0007 1846			1274+	VGM	V22, 0, 7, 1	test instruction (dest is a source)



LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00001C84	E760 5030 080E		00001C60	1275+	VST	V22, V1027	save v1 output
00001C8A	07FB			1276+	BR	R11	return
00001C8C				1277+RE27	DC	0F	xl16 expected result
00001C8C				1278+	DROP	R5	
00001C8C	FF00FF00 FF00FF00			1279	DC	XL16' FF00FF00FF00FF00 FF00FF00FF00FF00'	result t
00001C94	FF00FF00 FF00FF00						
				1280			
				1281	VRI_B	VGM 0, 8, 1	
00001CA0				1282+	DS	0FD	
00001CA0		00001CA0		1283+	USING	*, R5	base for test data and test routine
00001CA0	00001CE8			1284+T28	DC	A(X28)	address of test routine
00001CA4	001C			1285+	DC	H' 28'	test number
00001CA6	00			1286+	DC	X' 00'	
00001CA7	01			1287+	DC	HL1' 1'	M4 field
00001CA8	00			1288+	DC	HL1' 0'	i2 used
00001CA9	08			1289+	DC	HL1' 8'	i3 used
00001CAA	E5C7D440 40404040			1290+	DC	CL8' VGM	instruction name
00001CB4	00001D0C			1291+	DC	A(RE28+16)	address of v2 source
00001CB8	00001D1C			1292+	DC	A(RE28+32)	address of v3 source
00001CBC	00000010			1293+	DC	A(16)	result length
00001CC0	00001CFC			1294+REA28	DC	A(RE28)	result address
00001CC8	00000000 00000000			1295+	DS	FD	gap
00001CD0	00000000 00000000			1296+V1028	DS	XL16	V1 output
00001CD8	00000000 00000000						
00001CE0	00000000 00000000			1297+	DS	FD	gap
				1298+*			
00001CE8				1299+X28	DS	0F	
00001CE8	E760 8EAC 0806		000010AC	1300+	VL	V22, V1FUDGE	
00001CEE	E760 0008 1846			1301+	VGM	V22, 0, 8, 1	test instruction (dest is a source)
00001CF4	E760 5030 080E		00001CD0	1302+	VST	V22, V1028	save v1 output
00001CFA	07FB			1303+	BR	R11	return
00001CFC				1304+RE28	DC	0F	xl16 expected result
00001CFC				1305+	DROP	R5	
00001CFC	FF80FF80 FF80FF80			1306	DC	XL16' FF80FF80FF80FF80 FF80FF80FF80FF80'	result t
00001D04	FF80FF80 FF80FF80						
				1307			
				1308	VRI_B	VGM 0, 9, 1	
00001D10				1309+	DS	0FD	
00001D10		00001D10		1310+	USING	*, R5	base for test data and test routine
00001D10	00001D58			1311+T29	DC	A(X29)	address of test routine
00001D14	001D			1312+	DC	H' 29'	test number
00001D16	00			1313+	DC	X' 00'	
00001D17	01			1314+	DC	HL1' 1'	M4 field
00001D18	00			1315+	DC	HL1' 0'	i2 used
00001D19	09			1316+	DC	HL1' 9'	i3 used
00001D1A	E5C7D440 40404040			1317+	DC	CL8' VGM	instruction name
00001D24	00001D7C			1318+	DC	A(RE29+16)	address of v2 source
00001D28	00001D8C			1319+	DC	A(RE29+32)	address of v3 source
00001D2C	00000010			1320+	DC	A(16)	result length
00001D30	00001D6C			1321+REA29	DC	A(RE29)	result address
00001D38	00000000 00000000			1322+	DS	FD	gap
00001D40	00000000 00000000			1323+V1029	DS	XL16	V1 output
00001D48	00000000 00000000						
00001D50	00000000 00000000			1324+	DS	FD	gap
				1325+*			
00001D58				1326+X29	DS	0F	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00001D58	E760 8EAC 0806		000010AC	1327+	VL	V22, V1FUDGE	
00001D5E	E760 0009 1846			1328+	VGM	V22, 0, 9, 1	test instruction (dest is a source)
00001D64	E760 5030 080E		00001D40	1329+	VST	V22, V1029	save v1 output
00001D6A	07FB			1330+	BR	R11	return
00001D6C				1331+RE29	DC	0F	xl16 expected result
00001D6C				1332+	DROP	R5	
00001D6C	FFC0FFC0 FFC0FFC0			1333	DC	XL16' FFC0FFC0FFC0FFC0 FFC0FFC0FFC0FFC0'	result
00001D74	FFC0FFC0 FFC0FFC0						
				1334			
				1335	VRI_B	VGM 0, 11, 1	
00001D80				1336+	DS	0FD	
00001D80		00001D80		1337+	USING	*, R5	base for test data and test routine
00001D80	00001DC8			1338+T30	DC	A(X30)	address of test routine
00001D84	001E			1339+	DC	H' 30'	test number
00001D86	00			1340+	DC	X' 00'	
00001D87	01			1341+	DC	HL1' 1'	M4 field
00001D88	00			1342+	DC	HL1' 0'	i2 used
00001D89	0B			1343+	DC	HL1' 11'	i3 used
00001D8A	E5C7D440 40404040			1344+	DC	CL8' VGM	instruction name
00001D94	00001DEC			1345+	DC	A(RE30+16)	address of v2 source
00001D98	00001DFC			1346+	DC	A(RE30+32)	address of v3 source
00001D9C	00000010			1347+	DC	A(16)	result length
00001DA0	00001DDC			1348+REA30	DC	A(RE30)	result address
00001DA8	00000000 00000000			1349+	DS	FD	gap
00001DB0	00000000 00000000			1350+V1030	DS	XL16	V1 output
00001DB8	00000000 00000000						
00001DC0	00000000 00000000			1351+	DS	FD	gap
				1352+*			
00001DC8				1353+X30	DS	0F	
00001DC8	E760 8EAC 0806		000010AC	1354+	VL	V22, V1FUDGE	
00001DCE	E760 000B 1846			1355+	VGM	V22, 0, 11, 1	test instruction (dest is a source)
00001DD4	E760 5030 080E		00001DB0	1356+	VST	V22, V1030	save v1 output
00001DDA	07FB			1357+	BR	R11	return
00001DDC				1358+RE30	DC	0F	xl16 expected result
00001DDC				1359+	DROP	R5	
00001DDC	FFF0FFF0 FFF0FFF0			1360	DC	XL16' FFF0FFF0FFF0FFF0 FFF0FFF0FFF0FFF0'	result
00001DE4	FFF0FFF0 FFF0FFF0						
				1361			
				1362	VRI_B	VGM 0, 13, 1	
00001DF0				1363+	DS	0FD	
00001DF0		00001DF0		1364+	USING	*, R5	base for test data and test routine
00001DF0	00001E38			1365+T31	DC	A(X31)	address of test routine
00001DF4	001F			1366+	DC	H' 31'	test number
00001DF6	00			1367+	DC	X' 00'	
00001DF7	01			1368+	DC	HL1' 1'	M4 field
00001DF8	00			1369+	DC	HL1' 0'	i2 used
00001DF9	0D			1370+	DC	HL1' 13'	i3 used
00001DFA	E5C7D440 40404040			1371+	DC	CL8' VGM	instruction name
00001E04	00001E5C			1372+	DC	A(RE31+16)	address of v2 source
00001E08	00001E6C			1373+	DC	A(RE31+32)	address of v3 source
00001E0C	00000010			1374+	DC	A(16)	result length
00001E10	00001E4C			1375+REA31	DC	A(RE31)	result address
00001E18	00000000 00000000			1376+	DS	FD	gap
00001E20	00000000 00000000			1377+V1031	DS	XL16	V1 output
00001E28	00000000 00000000						
00001E30	00000000 00000000			1378+	DS	FD	gap

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00001E38				1379+*			
00001E38	E760 8EAC 0806		000010AC	1380+X31	DS	0F	
00001E3E	E760 000D 1846			1381+	VL	V22, V1FUDGE	
00001E44	E760 5030 080E		00001E20	1382+	VGM	V22, 0, 13, 1	test instruction (dest is a source)
00001E4A	07FB			1383+	VST	V22, V1031	save v1 output
00001E4C				1384+	BR	R11	return
00001E4C				1385+RE31	DC	0F	xl16 expected result
00001E4C	FFFCFFFC FFCFFFC			1386+	DROP	R5	
00001E4C	FFFCFFFC FFCFFFC			1387	DC	XL16' FFCFFFCFFFCFFFC FFCFFFCFFFCFFFC'	result
00001E54	FFFCFFFC FFCFFFC						
00001E60				1388			
00001E60		00001E60		1389	VRI_B	VGM 0, 15, 1	
00001E60	00001EA8			1390+	DS	0FD	
00001E64	0020			1391+	USING	*, R5	base for test data and test routine
00001E66	00			1392+T32	DC	A(X32)	address of test routine
00001E67	01			1393+	DC	H' 32'	test number
00001E68	00			1394+	DC	X' 00'	
00001E69	0F			1395+	DC	HL1' 1'	M4 field
00001E6A	E5C7D440 40404040			1396+	DC	HL1' 0'	i2 used
00001E74	00001ECC			1397+	DC	HL1' 15'	i3 used
00001E78	00001EDC			1398+	DC	CL8' VGM	instruction name
00001E7C	00000010			1399+	DC	A(RE32+16)	address of v2 source
00001E80	00001EBC			1400+	DC	A(RE32+32)	address of v3 source
00001E88	00000000 00000000			1401+	DC	A(16)	result length
00001E90	00000000 00000000			1402+REA32	DC	A(RE32)	result address
00001E98	00000000 00000000			1403+	DS	FD	gap
00001EA0	00000000 00000000			1404+V1032	DS	XL16	V1 output
00001EA8				1405+	DS	FD	gap
00001EA8	E760 8EAC 0806		000010AC	1406+*			
00001EAE	E760 000F 1846			1407+X32	DS	0F	
00001EB4	E760 5030 080E		00001E90	1408+	VL	V22, V1FUDGE	
00001EBA	07FB			1409+	VGM	V22, 0, 15, 1	test instruction (dest is a source)
00001EBC				1410+	VST	V22, V1032	save v1 output
00001EBC				1411+	BR	R11	return
00001EBC	FFFFFFFF FFFFFFFF			1412+RE32	DC	0F	xl16 expected result
00001EC4	FFFFFFFF FFFFFFFF			1413+	DROP	R5	
00001ED0				1414	DC	XL16' FFFFFFFF FFFFFFFF FFFFFFFF FFFFFFFF'	result
00001ED0				1415			
00001ED0	00001F18	00001ED0		1416	VRI_B	VGM 0, 16, 1	
00001ED4	0021			1417+	DS	0FD	
00001ED6	00			1418+	USING	*, R5	base for test data and test routine
00001ED7	01			1419+T33	DC	A(X33)	address of test routine
00001ED8	00			1420+	DC	H' 33'	test number
00001ED9	10			1421+	DC	X' 00'	
00001EDA	E5C7D440 40404040			1422+	DC	HL1' 1'	M4 field
00001EE4	00001F3C			1423+	DC	HL1' 0'	i2 used
00001EE8	00001F4C			1424+	DC	HL1' 16'	i3 used
00001EEC	00000010			1425+	DC	CL8' VGM	instruction name
00001EF0	00001F2C			1426+	DC	A(RE33+16)	address of v2 source
00001EF8	00000000 00000000			1427+	DC	A(RE33+32)	address of v3 source
00001F00	00000000 00000000			1428+	DC	A(16)	result length
				1429+REA33	DC	A(RE33)	result address
				1430+	DS	FD	gap
				1431+V1033	DS	XL16	V1 output



LOC	OBJECT CODE	ADDR1	ADDR2	STMT	
				1444 *Halfword: I2<I3; I2=1	
				1445 VRI_B VGM 1, 1, 1	
00001F40				1446+ DS OFD	
00001F40		00001F40		1447+ USING *, R5	base for test data and test routine
00001F40	00001F88			1448+T34 DC A(X34)	address of test routine
00001F44	0022			1449+ DC H' 34'	test number
00001F46	00			1450+ DC X' 00'	
00001F47	01			1451+ DC HL1' 1'	M4 field
00001F48	01			1452+ DC HL1' 1'	i2 used
00001F49	01			1453+ DC HL1' 1'	i3 used
00001F4A	E5C7D440 40404040			1454+ DC CL8' VGM	instruction name
00001F54	00001FAC			1455+ DC A(RE34+16)	address of v2 source
00001F58	00001FBC			1456+ DC A(RE34+32)	address of v3 source
00001F5C	00000010			1457+ DC A(16)	result length
00001F60	00001F9C			1458+REA34 DC A(RE34)	result address
00001F68	00000000 00000000			1459+ DS FD	gap
00001F70	00000000 00000000			1460+V1034 DS XL16	V1 output
00001F78	00000000 00000000				
00001F80	00000000 00000000			1461+ DS FD	gap
				1462+*	
00001F88				1463+X34 DS OF	
00001F88	E760 8EAC 0806		000010AC	1464+ VL V22, V1FUDGE	
00001F8E	E760 0101 1846			1465+ VGM V22, 1, 1, 1	test instruction (dest is a source)
00001F94	E760 5030 080E		00001F70	1466+ VST V22, V1034	save v1 output
00001F9A	07FB			1467+ BR R11	return
00001F9C				1468+RE34 DC OF	xl16 expected result
00001F9C				1469+ DROP R5	
00001F9C	40004000 40004000			1470 DC XL16' 4000400040004000 4000400040004000'	result t
00001FA4	40004000 40004000				
				1471	
				1472 VRI_B VGM 1, 2, 1	
00001FB0				1473+ DS OFD	
00001FB0		00001FB0		1474+ USING *, R5	base for test data and test routine
00001FB0	00001FF8			1475+T35 DC A(X35)	address of test routine
00001FB4	0023			1476+ DC H' 35'	test number
00001FB6	00			1477+ DC X' 00'	
00001FB7	01			1478+ DC HL1' 1'	M4 field
00001FB8	01			1479+ DC HL1' 1'	i2 used
00001FB9	02			1480+ DC HL1' 2'	i3 used
00001FBA	E5C7D440 40404040			1481+ DC CL8' VGM	instruction name
00001FC4	0000201C			1482+ DC A(RE35+16)	address of v2 source
00001FC8	0000202C			1483+ DC A(RE35+32)	address of v3 source
00001FCC	00000010			1484+ DC A(16)	result length
00001FD0	0000200C			1485+REA35 DC A(RE35)	result address
00001FD8	00000000 00000000			1486+ DS FD	gap
00001FE0	00000000 00000000			1487+V1035 DS XL16	V1 output
00001FE8	00000000 00000000				
00001FF0	00000000 00000000			1488+ DS FD	gap
				1489+*	
00001FF8				1490+X35 DS OF	
00001FF8	E760 8EAC 0806		000010AC	1491+ VL V22, V1FUDGE	
00001FFE	E760 0102 1846			1492+ VGM V22, 1, 2, 1	test instruction (dest is a source)
00002004	E760 5030 080E		00001FE0	1493+ VST V22, V1035	save v1 output
0000200A	07FB			1494+ BR R11	return
0000200C				1495+RE35 DC OF	xl16 expected result
0000200C				1496+ DROP R5	



LOC	OBJECT CODE	ADDR1	ADDR2	STMT					
0000200C	60006000 60006000			1497	DC	XL16' 6000600060006000 6000600060006000'	result		
00002014	60006000 60006000								
				1498					
				1499	VRI_B	VGM 1, 4, 1			
00002020				1500+	DS	OFD			
00002020		00002020		1501+	USING	*, R5	base for test data and test routine		
00002020	00002068			1502+T36	DC	A(X36)	address of test routine		
00002024	0024			1503+	DC	H' 36'	test number		
00002026	00			1504+	DC	X' 00'			
00002027	01			1505+	DC	HL1' 1'	M4 field		
00002028	01			1506+	DC	HL1' 1'	i2 used		
00002029	04			1507+	DC	HL1' 4'	i3 used		
0000202A	E5C7D440 40404040			1508+	DC	CL8' VGM	instruction name		
00002034	0000208C			1509+	DC	A(RE36+16)	address of v2 source		
00002038	0000209C			1510+	DC	A(RE36+32)	address of v3 source		
0000203C	00000010			1511+	DC	A(16)	result length		
00002040	0000207C			1512+REA36	DC	A(RE36)	result address		
00002048	00000000 00000000			1513+	DS	FD	gap		
00002050	00000000 00000000			1514+V1036	DS	XL16	V1 output		
00002058	00000000 00000000								
00002060	00000000 00000000			1515+	DS	FD	gap		
				1516+*					
00002068				1517+X36	DS	OF			
00002068	E760 8EAC 0806		000010AC	1518+	VL	V22, V1FUDGE			
0000206E	E760 0104 1846			1519+	VGM	V22, 1, 4, 1	test instruction (dest is a source)		
00002074	E760 5030 080E		00002050	1520+	VST	V22, V1036	save v1 output		
0000207A	07FB			1521+	BR	R11	return		
0000207C				1522+RE36	DC	OF	xl16 expected result		
0000207C				1523+	DROP	R5			
0000207C	78007800 78007800			1524	DC	XL16' 7800780078007800 7800780078007800'	result		
00002084	78007800 78007800								
				1525					
				1526	VRI_B	VGM 1, 6, 1			
00002090				1527+	DS	OFD			
00002090		00002090		1528+	USING	*, R5	base for test data and test routine		
00002090	000020D8			1529+T37	DC	A(X37)	address of test routine		
00002094	0025			1530+	DC	H' 37'	test number		
00002096	00			1531+	DC	X' 00'			
00002097	01			1532+	DC	HL1' 1'	M4 field		
00002098	01			1533+	DC	HL1' 1'	i2 used		
00002099	06			1534+	DC	HL1' 6'	i3 used		
0000209A	E5C7D440 40404040			1535+	DC	CL8' VGM	instruction name		
000020A4	000020FC			1536+	DC	A(RE37+16)	address of v2 source		
000020A8	0000210C			1537+	DC	A(RE37+32)	address of v3 source		
000020AC	00000010			1538+	DC	A(16)	result length		
000020B0	000020EC			1539+REA37	DC	A(RE37)	result address		
000020B8	00000000 00000000			1540+	DS	FD	gap		
000020C0	00000000 00000000			1541+V1037	DS	XL16	V1 output		
000020C8	00000000 00000000								
000020D0	00000000 00000000			1542+	DS	FD	gap		
				1543+*					
000020D8				1544+X37	DS	OF			
000020D8	E760 8EAC 0806		000010AC	1545+	VL	V22, V1FUDGE			
000020DE	E760 0106 1846			1546+	VGM	V22, 1, 6, 1	test instruction (dest is a source)		
000020E4	E760 5030 080E		000020C0	1547+	VST	V22, V1037	save v1 output		
000020EA	07FB			1548+	BR	R11	return		

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
000020EC				1549+RE37	DC	0F	xl16 expected result
000020EC				1550+	DROP	R5	
000020EC	7E007E00 7E007E00			1551	DC	XL16' 7E007E007E007E00 7E007E007E007E00'	result t
000020F4	7E007E00 7E007E00						
				1552			
				1553	VRI_B	VGM 1, 7, 1	
00002100				1554+	DS	0FD	
00002100		00002100		1555+	USING	*, R5	base for test data and test routine
00002100	00002148			1556+T38	DC	A(X38)	address of test routine
00002104	0026			1557+	DC	H' 38'	test number
00002106	00			1558+	DC	X' 00'	
00002107	01			1559+	DC	HL1' 1'	M4 field
00002108	01			1560+	DC	HL1' 1'	i2 used
00002109	07			1561+	DC	HL1' 7'	i3 used
0000210A	E5C7D440 40404040			1562+	DC	CL8' VGM	instruction name
00002114	0000216C			1563+	DC	A(RE38+16)	address of v2 source
00002118	0000217C			1564+	DC	A(RE38+32)	address of v3 source
0000211C	00000010			1565+	DC	A(16)	result length
00002120	0000215C			1566+REA38	DC	A(RE38)	result address
00002128	00000000 00000000			1567+	DS	FD	gap
00002130	00000000 00000000			1568+V1038	DS	XL16	V1 output
00002138	00000000 00000000						
00002140	00000000 00000000			1569+	DS	FD	gap
				1570+*			
00002148				1571+X38	DS	0F	
00002148	E760 8EAC 0806		000010AC	1572+	VL	V22, V1FUDGE	
0000214E	E760 0107 1846			1573+	VGM	V22, 1, 7, 1	test instruction (dest is a source)
00002154	E760 5030 080E		00002130	1574+	VST	V22, V1038	save v1 output
0000215A	07FB			1575+	BR	R11	return
0000215C				1576+RE38	DC	0F	xl16 expected result
0000215C				1577+	DROP	R5	
0000215C	7F007F00 7F007F00			1578	DC	XL16' 7F007F007F007F00 7F007F007F007F00'	result t
00002164	7F007F00 7F007F00						
				1579			
				1580	VRI_B	VGM 1, 8, 1	
00002170				1581+	DS	0FD	
00002170		00002170		1582+	USING	*, R5	base for test data and test routine
00002170	000021B8			1583+T39	DC	A(X39)	address of test routine
00002174	0027			1584+	DC	H' 39'	test number
00002176	00			1585+	DC	X' 00'	
00002177	01			1586+	DC	HL1' 1'	M4 field
00002178	01			1587+	DC	HL1' 1'	i2 used
00002179	08			1588+	DC	HL1' 8'	i3 used
0000217A	E5C7D440 40404040			1589+	DC	CL8' VGM	instruction name
00002184	000021DC			1590+	DC	A(RE39+16)	address of v2 source
00002188	000021EC			1591+	DC	A(RE39+32)	address of v3 source
0000218C	00000010			1592+	DC	A(16)	result length
00002190	000021CC			1593+REA39	DC	A(RE39)	result address
00002198	00000000 00000000			1594+	DS	FD	gap
000021A0	00000000 00000000			1595+V1039	DS	XL16	V1 output
000021A8	00000000 00000000						
000021B0	00000000 00000000			1596+	DS	FD	gap
				1597+*			
000021B8				1598+X39	DS	0F	
000021B8	E760 8EAC 0806		000010AC	1599+	VL	V22, V1FUDGE	
000021BE	E760 0108 1846			1600+	VGM	V22, 1, 8, 1	test instruction (dest is a source)



LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
000021C4	E760 5030 080E		000021A0	1601+	VST	V22, V1039	save v1 output
000021CA	07FB			1602+	BR	R11	return
000021CC				1603+RE39	DC	0F	xl16 expected result
000021CC				1604+	DROP	R5	
000021CC	7F807F80 7F807F80			1605	DC	XL16' 7F807F807F807F80 7F807F807F807F80'	result t
000021D4	7F807F80 7F807F80						
				1606			
				1607	VRI_B	VGM 1, 9, 1	
000021E0				1608+	DS	0FD	
000021E0		000021E0		1609+	USING	*, R5	base for test data and test routine
000021E0	00002228			1610+T40	DC	A(X40)	address of test routine
000021E4	0028			1611+	DC	H' 40'	test number
000021E6	00			1612+	DC	X' 00'	
000021E7	01			1613+	DC	HL1' 1'	M4 field
000021E8	01			1614+	DC	HL1' 1'	i2 used
000021E9	09			1615+	DC	HL1' 9'	i3 used
000021EA	E5C7D440 40404040			1616+	DC	CL8' VGM	instruction name
000021F4	0000224C			1617+	DC	A(RE40+16)	address of v2 source
000021F8	0000225C			1618+	DC	A(RE40+32)	address of v3 source
000021FC	00000010			1619+	DC	A(16)	result length
00002200	0000223C			1620+REA40	DC	A(RE40)	result address
00002208	00000000 00000000			1621+	DS	FD	gap
00002210	00000000 00000000			1622+V1040	DS	XL16	V1 output
00002218	00000000 00000000						
00002220	00000000 00000000			1623+	DS	FD	gap
				1624+*			
00002228				1625+X40	DS	0F	
00002228	E760 8EAC 0806		000010AC	1626+	VL	V22, V1FUDGE	
0000222E	E760 0109 1846			1627+	VGM	V22, 1, 9, 1	test instruction (dest is a source)
00002234	E760 A010 080E		00002210	1628+	VST	V22, V1040	save v1 output
0000223A	07FB			1629+	BR	R11	return
0000223C				1630+RE40	DC	0F	xl16 expected result
0000223C				1631+	DROP	R5	
0000223C	7FC07FC0 7FC07FC0			1632	DC	XL16' 7FC07FC07FC07FC0 7FC07FC07FC07FC0'	result t
00002244	7FC07FC0 7FC07FC0						
				1633			
				1634	VRI_B	VGM 1, 11, 1	
00002250				1635+	DS	0FD	
00002250		00002250		1636+	USING	*, R5	base for test data and test routine
00002250	00002298			1637+T41	DC	A(X41)	address of test routine
00002254	0029			1638+	DC	H' 41'	test number
00002256	00			1639+	DC	X' 00'	
00002257	01			1640+	DC	HL1' 1'	M4 field
00002258	01			1641+	DC	HL1' 1'	i2 used
00002259	0B			1642+	DC	HL1' 11'	i3 used
0000225A	E5C7D440 40404040			1643+	DC	CL8' VGM	instruction name
00002264	000022BC			1644+	DC	A(RE41+16)	address of v2 source
00002268	000022CC			1645+	DC	A(RE41+32)	address of v3 source
0000226C	00000010			1646+	DC	A(16)	result length
00002270	000022AC			1647+REA41	DC	A(RE41)	result address
00002278	00000000 00000000			1648+	DS	FD	gap
00002280	00000000 00000000			1649+V1041	DS	XL16	V1 output
00002288	00000000 00000000						
00002290	00000000 00000000			1650+	DS	FD	gap
				1651+*			
00002298				1652+X41	DS	0F	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00002298	E760 8EAC 0806		000010AC	1653+	VL	V22, V1FUDGE	
0000229E	E760 010B 1846			1654+	VGM	V22, 1, 11, 1	test instruction (dest is a source)
000022A4	E760 5030 080E		00002280	1655+	VST	V22, V1041	save v1 output
000022AA	07FB			1656+	BR	R11	return
000022AC				1657+RE41	DC	0F	xl16 expected result
000022AC				1658+	DROP	R5	
000022AC	7FF07FF0 7FF07FF0			1659	DC	XL16' 7FF07FF07FF07FF0 7FF07FF07FF07FF0'	result
000022B4	7FF07FF0 7FF07FF0						
				1660			
000022C0				1661	VRI_B	VGM 1, 13, 1	
000022C0		000022C0		1662+	DS	0FD	
000022C0	00002308			1663+	USING	*, R5	base for test data and test routine
000022C4	002A			1664+T42	DC	A(X42)	address of test routine
000022C6	00			1665+	DC	H' 42'	test number
000022C7	01			1666+	DC	X' 00'	
000022C8	01			1667+	DC	HL1' 1'	M4 field
000022C9	0D			1668+	DC	HL1' 1'	i2 used
000022CA	E5C7D440 40404040			1669+	DC	HL1' 13'	i3 used
000022D4	0000232C			1670+	DC	CL8' VGM	instruction name
000022D8	0000233C			1671+	DC	A(RE42+16)	address of v2 source
000022DC	00000010			1672+	DC	A(RE42+32)	address of v3 source
000022E0	0000231C			1673+	DC	A(16)	result length
000022E8	00000000 00000000			1674+REA42	DC	A(RE42)	result address
000022F0	00000000 00000000			1675+	DS	FD	gap
000022F8	00000000 00000000			1676+V1042	DS	XL16	V1 output
00002300	00000000 00000000			1677+	DS	FD	gap
				1678+*			
00002308				1679+X42	DS	0F	
00002308	E760 8EAC 0806		000010AC	1680+	VL	V22, V1FUDGE	
0000230E	E760 010D 1846			1681+	VGM	V22, 1, 13, 1	test instruction (dest is a source)
00002314	E760 5030 080E		000022F0	1682+	VST	V22, V1042	save v1 output
0000231A	07FB			1683+	BR	R11	return
0000231C				1684+RE42	DC	0F	xl16 expected result
0000231C				1685+	DROP	R5	
0000231C	7FFC7FFC 7FFC7FFC			1686	DC	XL16' 7FFC7FFC7FFC7FFC 7FFC7FFC7FFC7FFC'	result
00002324	7FFC7FFC 7FFC7FFC						
				1687			
00002330				1688	VRI_B	VGM 1, 15, 1	
00002330		00002330		1689+	DS	0FD	
00002330	00002378			1690+	USING	*, R5	base for test data and test routine
00002334	002B			1691+T43	DC	A(X43)	address of test routine
00002336	00			1692+	DC	H' 43'	test number
00002337	01			1693+	DC	X' 00'	
00002338	01			1694+	DC	HL1' 1'	M4 field
00002339	0F			1695+	DC	HL1' 1'	i2 used
0000233A	E5C7D440 40404040			1696+	DC	HL1' 15'	i3 used
00002344	0000239C			1697+	DC	CL8' VGM	instruction name
00002348	000023AC			1698+	DC	A(RE43+16)	address of v2 source
0000234C	00000010			1699+	DC	A(RE43+32)	address of v3 source
00002350	0000238C			1700+	DC	A(16)	result length
00002358	00000000 00000000			1701+REA43	DC	A(RE43)	result address
00002360	00000000 00000000			1702+	DS	FD	gap
00002368	00000000 00000000			1703+V1043	DS	XL16	V1 output
00002370	00000000 00000000			1704+	DS	FD	gap



LOC	OBJECT CODE	ADDR1	ADDR2	STMT	
				1743 *Halfword: I2>I3; I3=0	
				1744 VRI_B VGM 2, 0, 1	
00002410				1745+ DS OFD	
00002410		00002410		1746+ USING *, R5	base for test data and test routine
00002410	00002458			1747+T45 DC A(X45)	address of test routine
00002414	002D			1748+ DC H' 45'	test number
00002416	00			1749+ DC X' 00'	
00002417	01			1750+ DC HL1' 1'	M4 field
00002418	02			1751+ DC HL1' 2'	i2 used
00002419	00			1752+ DC HL1' 0'	i3 used
0000241A	E5C7D440 40404040			1753+ DC CL8' VGM	instruction name
00002424	0000247C			1754+ DC A(RE45+16)	address of v2 source
00002428	0000248C			1755+ DC A(RE45+32)	address of v3 source
0000242C	00000010			1756+ DC A(16)	result length
00002430	0000246C			1757+REA45 DC A(RE45)	result address
00002438	00000000 00000000			1758+ DS FD	gap
00002440	00000000 00000000			1759+V1045 DS XL16	V1 output
00002448	00000000 00000000				
00002450	00000000 00000000			1760+ DS FD	gap
				1761+*	
00002458				1762+X45 DS OF	
00002458	E760 8EAC 0806	000010AC		1763+ VL V22, V1FUDGE	
0000245E	E760 0200 1846			1764+ VGM V22, 2, 0, 1	test instruction (dest is a source)
00002464	E760 5030 080E	00002440		1765+ VST V22, V1045	save v1 output
0000246A	07FB			1766+ BR R11	return
0000246C				1767+RE45 DC OF	xl16 expected result
0000246C				1768+ DROP R5	
0000246C	BFFFBFFF BFFFBFFF			1769 DC XL16' BFFFBFFFBFFFBFFF BFFFBFFFBFFFBFFF'	result t
00002474	BFFFBFFF BFFFBFFF				
				1770	
				1771 VRI_B VGM 4, 0, 1	
00002480				1772+ DS OFD	
00002480		00002480		1773+ USING *, R5	base for test data and test routine
00002480	000024C8			1774+T46 DC A(X46)	address of test routine
00002484	002E			1775+ DC H' 46'	test number
00002486	00			1776+ DC X' 00'	
00002487	01			1777+ DC HL1' 1'	M4 field
00002488	04			1778+ DC HL1' 4'	i2 used
00002489	00			1779+ DC HL1' 0'	i3 used
0000248A	E5C7D440 40404040			1780+ DC CL8' VGM	instruction name
00002494	000024EC			1781+ DC A(RE46+16)	address of v2 source
00002498	000024FC			1782+ DC A(RE46+32)	address of v3 source
0000249C	00000010			1783+ DC A(16)	result length
000024A0	000024DC			1784+REA46 DC A(RE46)	result address
000024A8	00000000 00000000			1785+ DS FD	gap
000024B0	00000000 00000000			1786+V1046 DS XL16	V1 output
000024B8	00000000 00000000				
000024C0	00000000 00000000			1787+ DS FD	gap
				1788+*	
000024C8				1789+X46 DS OF	
000024C8	E760 8EAC 0806	000010AC		1790+ VL V22, V1FUDGE	
000024CE	E760 0400 1846			1791+ VGM V22, 4, 0, 1	test instruction (dest is a source)
000024D4	E760 5030 080E	000024B0		1792+ VST V22, V1046	save v1 output
000024DA	07FB			1793+ BR R11	return
000024DC				1794+RE46 DC OF	xl16 expected result
000024DC				1795+ DROP R5	



LOC	OBJECT CODE	ADDR1	ADDR2	STMT		
000024DC	8FFF8FFF 8FFF8FFF			1796	DC	XL16' 8FFF8FFF8FFF8FFF 8FFF8FFF8FFF8FFF' result t
000024E4	8FFF8FFF 8FFF8FFF					
				1797		
				1798	VRI_B	VGM 6, 0, 1
000024F0				1799+	DS	OFD
000024F0		000024F0		1800+	USING	*, R5
000024F0	00002538			1801+T47	DC	A(X47)
000024F4	002F			1802+	DC	H' 47'
000024F6	00			1803+	DC	X' 00'
000024F7	01			1804+	DC	HL1' 1'
000024F8	06			1805+	DC	HL1' 6'
000024F9	00			1806+	DC	HL1' 0'
000024FA	E5C7D440 40404040			1807+	DC	CL8' VGM
00002504	0000255C			1808+	DC	A(RE47+16)
00002508	0000256C			1809+	DC	A(RE47+32)
0000250C	00000010			1810+	DC	A(16)
00002510	0000254C			1811+REA47	DC	A(RE47)
00002518	00000000 00000000			1812+	DS	FD
00002520	00000000 00000000			1813+V1047	DS	XL16
00002528	00000000 00000000					
00002530	00000000 00000000			1814+	DS	FD
				1815+*		gap
00002538				1816+X47	DS	OF
00002538	E760 8EAC 0806		000010AC	1817+	VL	V22, V1FUDGE
0000253E	E760 0600 1846			1818+	VGM	V22, 6, 0, 1
00002544	E760 5030 080E		00002520	1819+	VST	V22, V1047
0000254A	07FB			1820+	BR	R11
0000254C				1821+RE47	DC	OF
0000254C				1822+	DROP	R5
0000254C	83FF83FF 83FF83FF			1823	DC	XL16' 83FF83FF83FF83FF 83FF83FF83FF83FF' result t
00002554	83FF83FF 83FF83FF					
				1824		
				1825	VRI_B	VGM 7, 0, 1
00002560				1826+	DS	OFD
00002560		00002560		1827+	USING	*, R5
00002560	000025A8			1828+T48	DC	A(X48)
00002564	0030			1829+	DC	H' 48'
00002566	00			1830+	DC	X' 00'
00002567	01			1831+	DC	HL1' 1'
00002568	07			1832+	DC	HL1' 7'
00002569	00			1833+	DC	HL1' 0'
0000256A	E5C7D440 40404040			1834+	DC	CL8' VGM
00002574	000025CC			1835+	DC	A(RE48+16)
00002578	000025DC			1836+	DC	A(RE48+32)
0000257C	00000010			1837+	DC	A(16)
00002580	000025BC			1838+REA48	DC	A(RE48)
00002588	00000000 00000000			1839+	DS	FD
00002590	00000000 00000000			1840+V1048	DS	XL16
00002598	00000000 00000000					
000025A0	00000000 00000000			1841+	DS	FD
				1842+*		gap
000025A8				1843+X48	DS	OF
000025A8	E760 8EAC 0806		000010AC	1844+	VL	V22, V1FUDGE
000025AE	E760 0700 1846			1845+	VGM	V22, 7, 0, 1
000025B4	E760 5030 080E		00002590	1846+	VST	V22, V1048
000025BA	07FB			1847+	BR	R11

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
000025BC				1848+RE48	DC	0F	xl16 expected result
000025BC				1849+	DROP	R5	
000025BC	81FF81FF 81FF81FF			1850	DC	XL16' 81FF81FF81FF81FF 81FF81FF81FF81FF'	result t
000025C4	81FF81FF 81FF81FF						
				1851			
000025D0				1852	VRI_B	VGM 8, 0, 1	
000025D0		000025D0		1853+	DS	0FD	
000025D0	00002618			1854+	USING	*, R5	base for test data and test routine
000025D4	0031			1855+T49	DC	A(X49)	address of test routine
000025D6	00			1856+	DC	H' 49'	test number
000025D7	01			1857+	DC	X' 00'	
000025D8	08			1858+	DC	HL1' 1'	M4 field
000025D9	00			1859+	DC	HL1' 8'	i2 used
000025DA	E5C7D440 40404040			1860+	DC	HL1' 0'	i3 used
000025E4	0000263C			1861+	DC	CL8' VGM	instruction name
000025E8	0000264C			1862+	DC	A(RE49+16)	address of v2 source
000025EC	00000010			1863+	DC	A(RE49+32)	address of v3 source
000025F0	0000262C			1864+	DC	A(16)	result length
000025F8	00000000 00000000			1865+REA49	DC	A(RE49)	result address
00002600	00000000 00000000			1866+	DS	FD	gap
00002608	00000000 00000000			1867+V1049	DS	XL16	V1 output
00002610	00000000 00000000			1868+	DS	FD	gap
				1869+*			
00002618				1870+X49	DS	0F	
00002618	E760 8EAC 0806		000010AC	1871+	VL	V22, V1FUDGE	
0000261E	E760 0800 1846			1872+	VGM	V22, 8, 0, 1	test instruction (dest is a source)
00002624	E760 5030 080E		00002600	1873+	VST	V22, V1049	save v1 output
0000262A	07FB			1874+	BR	R11	return
0000262C				1875+RE49	DC	0F	xl16 expected result
0000262C				1876+	DROP	R5	
0000262C	80FF80FF 80FF80FF			1877	DC	XL16' 80FF80FF80FF80FF 80FF80FF80FF80FF'	result t
00002634	80FF80FF 80FF80FF						
				1878			
00002640				1879	VRI_B	VGM 9, 0, 1	
00002640		00002640		1880+	DS	0FD	
00002640	00002688			1881+	USING	*, R5	base for test data and test routine
00002644	0032			1882+T50	DC	A(X50)	address of test routine
00002646	00			1883+	DC	H' 50'	test number
00002647	01			1884+	DC	X' 00'	
00002648	09			1885+	DC	HL1' 1'	M4 field
00002649	00			1886+	DC	HL1' 9'	i2 used
0000264A	E5C7D440 40404040			1887+	DC	HL1' 0'	i3 used
00002654	000026AC			1888+	DC	CL8' VGM	instruction name
00002658	000026BC			1889+	DC	A(RE50+16)	address of v2 source
0000265C	00000010			1890+	DC	A(RE50+32)	address of v3 source
00002660	0000269C			1891+	DC	A(16)	result length
00002668	00000000 00000000			1892+REA50	DC	A(RE50)	result address
00002670	00000000 00000000			1893+	DS	FD	gap
00002678	00000000 00000000			1894+V1050	DS	XL16	V1 output
00002680	00000000 00000000			1895+	DS	FD	gap
				1896+*			
00002688				1897+X50	DS	0F	
00002688	E760 8EAC 0806		000010AC	1898+	VL	V22, V1FUDGE	
0000268E	E760 0900 1846			1899+	VGM	V22, 9, 0, 1	test instruction (dest is a source)



LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00002694	E760 5030 080E		00002670	1900+	VST	V22, V1050	save v1 output
0000269A	07FB			1901+	BR	R11	return
0000269C				1902+RE50	DC	0F	xl16 expected result
0000269C				1903+	DROP	R5	
0000269C	807F807F 807F807F			1904	DC	XL16' 807F807F807F807F 807F807F807F807F'	result t
000026A4	807F807F 807F807F						
				1905			
				1906	VRI_B	VGM, 11, 0, 1	
000026B0				1907+	DS	0FD	
000026B0		000026B0		1908+	USING	*, R5	base for test data and test routine
000026B0	000026F8			1909+T51	DC	A(X51)	address of test routine
000026B4	0033			1910+	DC	H' 51'	test number
000026B6	00			1911+	DC	X' 00'	
000026B7	01			1912+	DC	HL1' 1'	M4 field
000026B8	0B			1913+	DC	HL1' 11'	i2 used
000026B9	00			1914+	DC	HL1' 0'	i3 used
000026BA	E5C7D440 40404040			1915+	DC	CL8' VGM	instruction name
000026C4	0000271C			1916+	DC	A(RE51+16)	address of v2 source
000026C8	0000272C			1917+	DC	A(RE51+32)	address of v3 source
000026CC	00000010			1918+	DC	A(16)	result length
000026D0	0000270C			1919+REA51	DC	A(RE51)	result address
000026D8	00000000 00000000			1920+	DS	FD	gap
000026E0	00000000 00000000			1921+V1051	DS	XL16	V1 output
000026E8	00000000 00000000						
000026F0	00000000 00000000			1922+	DS	FD	gap
				1923+*			
000026F8				1924+X51	DS	0F	
000026F8	E760 8EAC 0806		000010AC	1925+	VL	V22, V1FUDGE	
000026FE	E760 0B00 1846			1926+	VGM	V22, 11, 0, 1	test instruction (dest is a source)
00002704	E760 5030 080E		000026E0	1927+	VST	V22, V1051	save v1 output
0000270A	07FB			1928+	BR	R11	return
0000270C				1929+RE51	DC	0F	xl16 expected result
0000270C				1930+	DROP	R5	
0000270C	801F801F 801F801F			1931	DC	XL16' 801F801F801F801F 801F801F801F801F'	result t
00002714	801F801F 801F801F						
				1932			
				1933	VRI_B	VGM, 13, 0, 1	
00002720				1934+	DS	0FD	
00002720		00002720		1935+	USING	*, R5	base for test data and test routine
00002720	00002768			1936+T52	DC	A(X52)	address of test routine
00002724	0034			1937+	DC	H' 52'	test number
00002726	00			1938+	DC	X' 00'	
00002727	01			1939+	DC	HL1' 1'	M4 field
00002728	0D			1940+	DC	HL1' 13'	i2 used
00002729	00			1941+	DC	HL1' 0'	i3 used
0000272A	E5C7D440 40404040			1942+	DC	CL8' VGM	instruction name
00002734	0000278C			1943+	DC	A(RE52+16)	address of v2 source
00002738	0000279C			1944+	DC	A(RE52+32)	address of v3 source
0000273C	00000010			1945+	DC	A(16)	result length
00002740	0000277C			1946+REA52	DC	A(RE52)	result address
00002748	00000000 00000000			1947+	DS	FD	gap
00002750	00000000 00000000			1948+V1052	DS	XL16	V1 output
00002758	00000000 00000000						
00002760	00000000 00000000			1949+	DS	FD	gap
				1950+*			
00002768				1951+X52	DS	0F	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00002768	E760 8EAC 0806		000010AC	1952+	VL	V22, V1FUDGE	
0000276E	E760 0D00 1846			1953+	VGM	V22, 13, 0, 1	test instruction (dest is a source)
00002774	E760 5030 080E		00002750	1954+	VST	V22, V1052	save v1 output
0000277A	07FB			1955+	BR	R11	return
0000277C				1956+RE52	DC	0F	xl16 expected result
0000277C				1957+	DROP	R5	
0000277C	80078007 80078007			1958	DC	XL16' 8007800780078007 8007800780078007'	result
00002784	80078007 80078007						
				1959			
00002790				1960	VRI_B	VGM, 15, 0, 1	
00002790		00002790		1961+	DS	0FD	
00002790	000027D8			1962+	USING	*, R5	base for test data and test routine
00002794	0035			1963+T53	DC	A(X53)	address of test routine
00002796	00			1964+	DC	H' 53'	test number
00002797	01			1965+	DC	X' 00'	
00002797	01			1966+	DC	HL1' 1'	M4 field
00002798	0F			1967+	DC	HL1' 15'	i2 used
00002799	00			1968+	DC	HL1' 0'	i3 used
0000279A	E5C7D440 40404040			1969+	DC	CL8' VGM	instruction name
000027A4	000027FC			1970+	DC	A(RE53+16)	address of v2 source
000027A8	0000280C			1971+	DC	A(RE53+32)	address of v3 source
000027AC	00000010			1972+	DC	A(16)	result length
000027B0	000027EC			1973+REA53	DC	A(RE53)	result address
000027B8	00000000 00000000			1974+	DS	FD	gap
000027C0	00000000 00000000			1975+V1053	DS	XL16	V1 output
000027C8	00000000 00000000						
000027D0	00000000 00000000			1976+	DS	FD	gap
				1977+*			
000027D8				1978+X53	DS	0F	
000027D8	E760 8EAC 0806		000010AC	1979+	VL	V22, V1FUDGE	
000027DE	E760 0F00 1846			1980+	VGM	V22, 15, 0, 1	test instruction (dest is a source)
000027E4	E760 5030 080E		000027C0	1981+	VST	V22, V1053	save v1 output
000027EA	07FB			1982+	BR	R11	return
000027EC				1983+RE53	DC	0F	xl16 expected result
000027EC				1984+	DROP	R5	
000027EC	80018001 80018001			1985	DC	XL16' 8001800180018001 8001800180018001'	result
000027F4	80018001 80018001						
				1986			
00002800				1987	VRI_B	VGM, 16, 0, 1	
00002800		00002800		1988+	DS	0FD	
00002800	00002848			1989+	USING	*, R5	base for test data and test routine
00002800	00002848			1990+T54	DC	A(X54)	address of test routine
00002804	0036			1991+	DC	H' 54'	test number
00002806	00			1992+	DC	X' 00'	
00002807	01			1993+	DC	HL1' 1'	M4 field
00002808	10			1994+	DC	HL1' 16'	i2 used
00002809	00			1995+	DC	HL1' 0'	i3 used
0000280A	E5C7D440 40404040			1996+	DC	CL8' VGM	instruction name
00002814	0000286C			1997+	DC	A(RE54+16)	address of v2 source
00002818	0000287C			1998+	DC	A(RE54+32)	address of v3 source
0000281C	00000010			1999+	DC	A(16)	result length
00002820	0000285C			2000+REA54	DC	A(RE54)	result address
00002828	00000000 00000000			2001+	DS	FD	gap
00002830	00000000 00000000			2002+V1054	DS	XL16	V1 output
00002838	00000000 00000000						
00002840	00000000 00000000			2003+	DS	FD	gap



LOC	OBJECT CODE	ADDR1	ADDR2	STMT	
				2015 *Halfword: I2>I3; I3=1	
				2016 VRI_B VGM 2, 1, 1	
00002870				2017+ DS OFD	
00002870		00002870		2018+ USING *, R5	base for test data and test routine
00002870	000028B8			2019+T55 DC A(X55)	address of test routine
00002874	0037			2020+ DC H' 55'	test number
00002876	00			2021+ DC X' 00'	
00002877	01			2022+ DC HL1' 1'	M4 field
00002878	02			2023+ DC HL1' 2'	i2 used
00002879	01			2024+ DC HL1' 1'	i3 used
0000287A	E5C7D440 40404040			2025+ DC CL8' VGM	instruction name
00002884	000028DC			2026+ DC A(RE55+16)	address of v2 source
00002888	000028EC			2027+ DC A(RE55+32)	address of v3 source
0000288C	00000010			2028+ DC A(16)	result length
00002890	000028CC			2029+REA55 DC A(RE55)	result address
00002898	00000000 00000000			2030+ DS FD	gap
000028A0	00000000 00000000			2031+V1055 DS XL16	V1 output
000028A8	00000000 00000000				
000028B0	00000000 00000000			2032+ DS FD	gap
				2033+*	
000028B8				2034+X55 DS OF	
000028B8	E760 8EAC 0806	000010AC		2035+ VL V22, V1FUDGE	
000028BE	E760 0201 1846			2036+ VGM V22, 2, 1, 1	test instruction (dest is a source)
000028C4	E760 5030 080E	000028A0		2037+ VST V22, V1055	save v1 output
000028CA	07FB			2038+ BR R11	return
000028CC				2039+RE55 DC OF	xl16 expected result
000028CC				2040+ DROP R5	
000028CC	FFFFFFFF FFFFFFFF			2041 DC XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF'	result t
000028D4	FFFFFFFF FFFFFFFF				
				2042	
				2043 VRI_B VGM 4, 1, 1	
000028E0				2044+ DS OFD	
000028E0		000028E0		2045+ USING *, R5	base for test data and test routine
000028E0	00002928			2046+T56 DC A(X56)	address of test routine
000028E4	0038			2047+ DC H' 56'	test number
000028E6	00			2048+ DC X' 00'	
000028E7	01			2049+ DC HL1' 1'	M4 field
000028E8	04			2050+ DC HL1' 4'	i2 used
000028E9	01			2051+ DC HL1' 1'	i3 used
000028EA	E5C7D440 40404040			2052+ DC CL8' VGM	instruction name
000028F4	0000294C			2053+ DC A(RE56+16)	address of v2 source
000028F8	0000295C			2054+ DC A(RE56+32)	address of v3 source
000028FC	00000010			2055+ DC A(16)	result length
00002900	0000293C			2056+REA56 DC A(RE56)	result address
00002908	00000000 00000000			2057+ DS FD	gap
00002910	00000000 00000000			2058+V1056 DS XL16	V1 output
00002918	00000000 00000000				
00002920	00000000 00000000			2059+ DS FD	gap
				2060+*	
00002928				2061+X56 DS OF	
00002928	E760 8EAC 0806	000010AC		2062+ VL V22, V1FUDGE	
0000292E	E760 0401 1846			2063+ VGM V22, 4, 1, 1	test instruction (dest is a source)
00002934	E760 5030 080E	00002910		2064+ VST V22, V1056	save v1 output
0000293A	07FB			2065+ BR R11	return
0000293C				2066+RE56 DC OF	xl16 expected result
0000293C				2067+ DROP R5	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
0000293C	CFFFCFFF CFFFCFFF			2068	DC	XL16' CFFFCFFFCFFFCFFF CFFFCFFFCFFFCFFF'	result t
00002944	CFFFCFFF CFFFCFFF						
				2069			
00002950				2070	VRI_B	VGM 6, 1, 1	
00002950		00002950		2071+	DS	OFD	
00002950	00002998			2072+	USING	*, R5	base for test data and test routine
00002954	0039			2073+T57	DC	A(X57)	address of test routine
00002956	00			2074+	DC	H' 57'	test number
00002957	01			2075+	DC	X' 00'	
00002958	06			2076+	DC	HL1' 1'	M4 field
00002959	01			2077+	DC	HL1' 6'	i2 used
0000295A	E5C7D440 40404040			2078+	DC	HL1' 1'	i3 used
00002964	000029BC			2079+	DC	CL8' VGM	instruction name
00002968	000029CC			2080+	DC	A(RE57+16)	address of v2 source
0000296C	00000010			2081+	DC	A(RE57+32)	address of v3 source
00002970	000029AC			2082+	DC	A(16)	result length
00002978	00000000 00000000			2083+REA57	DC	A(RE57)	result address
00002980	00000000 00000000			2084+	DS	FD	gap
00002988	00000000 00000000			2085+V1057	DS	XL16	V1 output
00002990	00000000 00000000						
				2086+	DS	FD	gap
				2087+*			
00002998				2088+X57	DS	OF	
00002998	E760 8EAC 0806		000010AC	2089+	VL	V22, V1FUDGE	
0000299E	E760 0601 1846			2090+	VGM	V22, 6, 1, 1	test instruction (dest is a source)
000029A4	E760 5030 080E		00002980	2091+	VST	V22, V1057	save v1 output
000029AA	07FB			2092+	BR	R11	return
000029AC				2093+RE57	DC	OF	xl16 expected result
000029AC				2094+	DROP	R5	
000029AC	C3FFC3FF C3FFC3FF			2095	DC	XL16' C3FFC3FFC3FFC3FF C3FFC3FFC3FFC3FF'	result t
000029B4	C3FFC3FF C3FFC3FF						
				2096			
000029C0				2097	VRI_B	VGM 7, 1, 1	
000029C0		000029C0		2098+	DS	OFD	
000029C0	00002A08			2099+	USING	*, R5	base for test data and test routine
000029C4	003A			2100+T58	DC	A(X58)	address of test routine
000029C6	00			2101+	DC	H' 58'	test number
000029C7	01			2102+	DC	X' 00'	
000029C8	07			2103+	DC	HL1' 1'	M4 field
000029C9	01			2104+	DC	HL1' 7'	i2 used
000029CA	E5C7D440 40404040			2105+	DC	HL1' 1'	i3 used
000029D4	00002A2C			2106+	DC	CL8' VGM	instruction name
000029D8	00002A3C			2107+	DC	A(RE58+16)	address of v2 source
000029DC	00000010			2108+	DC	A(RE58+32)	address of v3 source
000029E0	00002A1C			2109+	DC	A(16)	result length
000029E8	00000000 00000000			2110+REA58	DC	A(RE58)	result address
000029F0	00000000 00000000			2111+	DS	FD	gap
000029F8	00000000 00000000			2112+V1058	DS	XL16	V1 output
00002A00	00000000 00000000						
				2113+	DS	FD	gap
				2114+*			
00002A08				2115+X58	DS	OF	
00002A08	E760 8EAC 0806		000010AC	2116+	VL	V22, V1FUDGE	
00002A0E	E760 0701 1846			2117+	VGM	V22, 7, 1, 1	test instruction (dest is a source)
00002A14	E760 5030 080E		000029F0	2118+	VST	V22, V1058	save v1 output
00002A1A	07FB			2119+	BR	R11	return



LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00002A1C				2120+RE58	DC	0F	xl16 expected result
00002A1C				2121+	DROP	R5	
00002A1C	C1FFC1FF C1FFC1FF			2122	DC	XL16' C1FFC1FFC1FFC1FF C1FFC1FFC1FFC1FF'	result t
00002A24	C1FFC1FF C1FFC1FF						
				2123			
00002A30				2124	VRI_B	VGM 8, 1, 1	
00002A30		00002A30		2125+	DS	0FD	
00002A30	00002A78			2126+	USING	*, R5	base for test data and test routine
00002A34	003B			2127+T59	DC	A(X59)	address of test routine
00002A36	00			2128+	DC	H' 59'	test number
00002A37	01			2129+	DC	X' 00'	
00002A38	08			2130+	DC	HL1' 1'	M4 field
00002A39	01			2131+	DC	HL1' 8'	i2 used
00002A3A	E5C7D440 40404040			2132+	DC	HL1' 1'	i3 used
00002A44	00002A9C			2133+	DC	CL8' VGM	instruction name
00002A48	00002AAC			2134+	DC	A(RE59+16)	address of v2 source
00002A4C	00000010			2135+	DC	A(RE59+32)	address of v3 source
00002A50	00002A8C			2136+	DC	A(16)	result length
00002A58	00000000 00000000			2137+REA59	DC	A(RE59)	result address
00002A60	00000000 00000000			2138+	DS	FD	gap
00002A68	00000000 00000000			2139+V1059	DS	XL16	V1 output
00002A70	00000000 00000000			2140+	DS	FD	gap
				2141+*			
00002A78				2142+X59	DS	0F	
00002A78	E760 8EAC 0806		000010AC	2143+	VL	V22, V1FUDGE	
00002A7E	E760 0801 1846			2144+	VGM	V22, 8, 1, 1	test instruction (dest is a source)
00002A84	E760 5030 080E		00002A60	2145+	VST	V22, V1059	save v1 output
00002A8A	07FB			2146+	BR	R11	return
00002A8C				2147+RE59	DC	0F	xl16 expected result
00002A8C				2148+	DROP	R5	
00002A8C	COFFCOFF COFFCOFF			2149	DC	XL16' COFFCOFFCOFFCOFF COFFCOFFCOFFCOFF'	result t
00002A94	COFFCOFF COFFCOFF						
				2150			
00002AA0				2151	VRI_B	VGM 9, 1, 1	
00002AA0		00002AA0		2152+	DS	0FD	
00002AA0	00002AE8			2153+	USING	*, R5	base for test data and test routine
00002AA4	003C			2154+T60	DC	A(X60)	address of test routine
00002AA6	00			2155+	DC	H' 60'	test number
00002AA7	01			2156+	DC	X' 00'	
00002AA8	09			2157+	DC	HL1' 1'	M4 field
00002AA9	01			2158+	DC	HL1' 9'	i2 used
00002AAA	E5C7D440 40404040			2159+	DC	HL1' 1'	i3 used
00002AB4	00002B0C			2160+	DC	CL8' VGM	instruction name
00002AB8	00002B1C			2161+	DC	A(RE60+16)	address of v2 source
00002ABC	00000010			2162+	DC	A(RE60+32)	address of v3 source
00002AC0	00002AFC			2163+	DC	A(16)	result length
00002AC8	00000000 00000000			2164+REA60	DC	A(RE60)	result address
00002AD0	00000000 00000000			2165+	DS	FD	gap
00002AD8	00000000 00000000			2166+V1060	DS	XL16	V1 output
00002AE0	00000000 00000000						
				2167+	DS	FD	gap
				2168+*			
00002AE8				2169+X60	DS	0F	
00002AE8	E760 8EAC 0806		000010AC	2170+	VL	V22, V1FUDGE	
00002AEE	E760 0901 1846			2171+	VGM	V22, 9, 1, 1	test instruction (dest is a source)



LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00002AF4	E760 5030 080E		00002AD0	2172+	VST	V22, V1060	save v1 output
00002AFA	07FB			2173+	BR	R11	return
00002AFC				2174+RE60	DC	0F	xl16 expected result
00002AFC				2175+	DROP	R5	
00002AFC	C07FC07F C07FC07F			2176	DC	XL16' C07FC07FC07FC07F C07FC07FC07FC07F'	result t
00002B04	C07FC07F C07FC07F						
				2177			
				2178	VRI_B	VGM, 11, 1, 1	
00002B10				2179+	DS	0FD	
00002B10		00002B10		2180+	USING	*, R5	base for test data and test routine
00002B10	00002B58			2181+T61	DC	A(X61)	address of test routine
00002B14	003D			2182+	DC	H' 61'	test number
00002B16	00			2183+	DC	X' 00'	
00002B17	01			2184+	DC	HL1' 1'	M4 field
00002B18	0B			2185+	DC	HL1' 11'	i2 used
00002B19	01			2186+	DC	HL1' 1'	i3 used
00002B1A	E5C7D440 40404040			2187+	DC	CL8' VGM	instruction name
00002B24	00002B7C			2188+	DC	A(RE61+16)	address of v2 source
00002B28	00002B8C			2189+	DC	A(RE61+32)	address of v3 source
00002B2C	00000010			2190+	DC	A(16)	result length
00002B30	00002B6C			2191+REA61	DC	A(RE61)	result address
00002B38	00000000 00000000			2192+	DS	FD	gap
00002B40	00000000 00000000			2193+V1061	DS	XL16	V1 output
00002B48	00000000 00000000						
00002B50	00000000 00000000			2194+	DS	FD	gap
				2195+*			
00002B58				2196+X61	DS	0F	
00002B58	E760 8EAC 0806		000010AC	2197+	VL	V22, V1FUDGE	
00002B5E	E760 0B01 1846			2198+	VGM	V22, 11, 1, 1	test instruction (dest is a source)
00002B64	E760 5030 080E		00002B40	2199+	VST	V22, V1061	save v1 output
00002B6A	07FB			2200+	BR	R11	return
00002B6C				2201+RE61	DC	0F	xl16 expected result
00002B6C				2202+	DROP	R5	
00002B6C	C01FC01F C01FC01F			2203	DC	XL16' C01FC01FC01FC01F C01FC01FC01FC01F'	result t
00002B74	C01FC01F C01FC01F						
				2204			
				2205	VRI_B	VGM, 13, 1, 1	
00002B80				2206+	DS	0FD	
00002B80		00002B80		2207+	USING	*, R5	base for test data and test routine
00002B80	00002BC8			2208+T62	DC	A(X62)	address of test routine
00002B84	003E			2209+	DC	H' 62'	test number
00002B86	00			2210+	DC	X' 00'	
00002B87	01			2211+	DC	HL1' 1'	M4 field
00002B88	0D			2212+	DC	HL1' 13'	i2 used
00002B89	01			2213+	DC	HL1' 1'	i3 used
00002B8A	E5C7D440 40404040			2214+	DC	CL8' VGM	instruction name
00002B94	00002BEC			2215+	DC	A(RE62+16)	address of v2 source
00002B98	00002BFC			2216+	DC	A(RE62+32)	address of v3 source
00002B9C	00000010			2217+	DC	A(16)	result length
00002BA0	00002BDC			2218+REA62	DC	A(RE62)	result address
00002BA8	00000000 00000000			2219+	DS	FD	gap
00002BB0	00000000 00000000			2220+V1062	DS	XL16	V1 output
00002BB8	00000000 00000000						
00002BC0	00000000 00000000			2221+	DS	FD	gap
				2222+*			
00002BC8				2223+X62	DS	0F	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00002BC8	E760 8EAC 0806		000010AC	2224+	VL	V22, V1FUDGE	
00002BCE	E760 0D01 1846			2225+	VGM	V22, 13, 1, 1	test instruction (dest is a source)
00002BD4	E760 5030 080E		00002BB0	2226+	VST	V22, V1062	save v1 output
00002BDA	07FB			2227+	BR	R11	return
00002BDC				2228+RE62	DC	0F	xl16 expected result
00002BDC				2229+	DROP	R5	
00002BDC	C007C007 C007C007			2230	DC	XL16' C007C007C007C007 C007C007C007C007'	result
00002BE4	C007C007 C007C007						
				2231			
				2232	VRI_B	VGM, 15, 1, 1	
00002BF0				2233+	DS	0FD	
00002BF0		00002BF0		2234+	USING	*, R5	base for test data and test routine
00002BF0	00002C38			2235+T63	DC	A(X63)	address of test routine
00002BF4	003F			2236+	DC	H' 63'	test number
00002BF6	00			2237+	DC	X' 00'	
00002BF7	01			2238+	DC	HL1' 1'	M4 field
00002BF8	0F			2239+	DC	HL1' 15'	i2 used
00002BF9	01			2240+	DC	HL1' 1'	i3 used
00002BFA	E5C7D440 40404040			2241+	DC	CL8' VGM	instruction name
00002C04	00002C5C			2242+	DC	A(RE63+16)	address of v2 source
00002C08	00002C6C			2243+	DC	A(RE63+32)	address of v3 source
00002C0C	00000010			2244+	DC	A(16)	result length
00002C10	00002C4C			2245+REA63	DC	A(RE63)	result address
00002C18	00000000 00000000			2246+	DS	FD	gap
00002C20	00000000 00000000			2247+V1063	DS	XL16	V1 output
00002C28	00000000 00000000						
00002C30	00000000 00000000			2248+	DS	FD	gap
				2249+*			
00002C38				2250+X63	DS	0F	
00002C38	E760 8EAC 0806		000010AC	2251+	VL	V22, V1FUDGE	
00002C3E	E760 0F01 1846			2252+	VGM	V22, 15, 1, 1	test instruction (dest is a source)
00002C44	E760 5030 080E		00002C20	2253+	VST	V22, V1063	save v1 output
00002C4A	07FB			2254+	BR	R11	return
00002C4C				2255+RE63	DC	0F	xl16 expected result
00002C4C				2256+	DROP	R5	
00002C4C	C001C001 C001C001			2257	DC	XL16' C001C001C001C001 C001C001C001C001'	result
00002C54	C001C001 C001C001						
				2258			
				2259	VRI_B	VGM, 16, 1, 1	
00002C60				2260+	DS	0FD	
00002C60		00002C60		2261+	USING	*, R5	base for test data and test routine
00002C60	00002CA8			2262+T64	DC	A(X64)	address of test routine
00002C64	0040			2263+	DC	H' 64'	test number
00002C66	00			2264+	DC	X' 00'	
00002C67	01			2265+	DC	HL1' 1'	M4 field
00002C68	10			2266+	DC	HL1' 16'	i2 used
00002C69	01			2267+	DC	HL1' 1'	i3 used
00002C6A	E5C7D440 40404040			2268+	DC	CL8' VGM	instruction name
00002C74	00002CCC			2269+	DC	A(RE64+16)	address of v2 source
00002C78	00002CDC			2270+	DC	A(RE64+32)	address of v3 source
00002C7C	00000010			2271+	DC	A(16)	result length
00002C80	00002CBC			2272+REA64	DC	A(RE64)	result address
00002C88	00000000 00000000			2273+	DS	FD	gap
00002C90	00000000 00000000			2274+V1064	DS	XL16	V1 output
00002C98	00000000 00000000						
00002CA0	00000000 00000000			2275+	DS	FD	gap



LOC	OBJECT CODE	ADDR1	ADDR2	STMT	
				2314 *Word: I2<I3; I2=0	
				2315 VRI_B VGM 0, 0, 2	
00002D40				2316+ DS OFD	
00002D40		00002D40		2317+ USING *, R5	base for test data and test routine
00002D40	00002D88			2318+T66 DC A(X66)	address of test routine
00002D44	0042			2319+ DC H' 66'	test number
00002D46	00			2320+ DC X' 00'	
00002D47	02			2321+ DC HL1' 2'	M4 field
00002D48	00			2322+ DC HL1' 0'	i2 used
00002D49	00			2323+ DC HL1' 0'	i3 used
00002D4A	E5C7D440 40404040			2324+ DC CL8' VGM	instruction name
00002D54	00002DAC			2325+ DC A(RE66+16)	address of v2 source
00002D58	00002DBC			2326+ DC A(RE66+32)	address of v3 source
00002D5C	00000010			2327+ DC A(16)	result length
00002D60	00002D9C			2328+REA66 DC A(RE66)	result address
00002D68	00000000 00000000			2329+ DS FD	gap
00002D70	00000000 00000000			2330+V1066 DS XL16	V1 output
00002D78	00000000 00000000				
00002D80	00000000 00000000			2331+ DS FD	gap
				2332+*	
00002D88				2333+X66 DS OF	
00002D88	E760 8EAC 0806	000010AC		2334+ VL V22, V1FUDGE	
00002D8E	E760 0000 2846			2335+ VGM V22, 0, 0, 2	test instruction (dest is a source)
00002D94	E760 5030 080E	00002D70		2336+ VST V22, V1066	save v1 output
00002D9A	07FB			2337+ BR R11	return
00002D9C				2338+RE66 DC OF	xl16 expected result
00002D9C				2339+ DROP R5	
00002D9C	80000000 80000000			2340 DC XL16' 8000000080000000 8000000080000000'	result t
00002DA4	80000000 80000000				
				2341	
				2342 VRI_B VGM 0, 1, 2	
00002DB0				2343+ DS OFD	
00002DB0		00002DB0		2344+ USING *, R5	base for test data and test routine
00002DB0	00002DF8			2345+T67 DC A(X67)	address of test routine
00002DB4	0043			2346+ DC H' 67'	test number
00002DB6	00			2347+ DC X' 00'	
00002DB7	02			2348+ DC HL1' 2'	M4 field
00002DB8	00			2349+ DC HL1' 0'	i2 used
00002DB9	01			2350+ DC HL1' 1'	i3 used
00002DBA	E5C7D440 40404040			2351+ DC CL8' VGM	instruction name
00002DC4	00002E1C			2352+ DC A(RE67+16)	address of v2 source
00002DC8	00002E2C			2353+ DC A(RE67+32)	address of v3 source
00002DCC	00000010			2354+ DC A(16)	result length
00002DD0	00002E0C			2355+REA67 DC A(RE67)	result address
00002DD8	00000000 00000000			2356+ DS FD	gap
00002DE0	00000000 00000000			2357+V1067 DS XL16	V1 output
00002DE8	00000000 00000000				
00002DF0	00000000 00000000			2358+ DS FD	gap
				2359+*	
00002DF8				2360+X67 DS OF	
00002DF8	E760 8EAC 0806	000010AC		2361+ VL V22, V1FUDGE	
00002DFE	E760 0001 2846			2362+ VGM V22, 0, 1, 2	test instruction (dest is a source)
00002E04	E760 5030 080E	00002DE0		2363+ VST V22, V1067	save v1 output
00002E0A	07FB			2364+ BR R11	return
00002E0C				2365+RE67 DC OF	xl16 expected result
00002E0C				2366+ DROP R5	



LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00002E0C	C0000000 C0000000			2367	DC	XL16' C0000000C0000000 C0000000C0000000'	result
00002E14	C0000000 C0000000						
				2368			
00002E20				2369	VRI_B	VGM 0, 2, 2	
00002E20		00002E20		2370+	DS	OFD	
00002E20	00002E68			2371+	USING	*, R5	base for test data and test routine
00002E24	0044			2372+T68	DC	A(X68)	address of test routine
00002E26	00			2373+	DC	H' 68'	test number
00002E27	02			2374+	DC	X' 00'	
00002E28	00			2375+	DC	HL1' 2'	M4 field
00002E29	02			2376+	DC	HL1' 0'	i2 used
00002E2A	E5C7D440 40404040			2377+	DC	HL1' 2'	i3 used
00002E34	00002E8C			2378+	DC	CL8' VGM	instruction name
00002E38	00002E9C			2379+	DC	A(RE68+16)	address of v2 source
00002E3C	00000010			2380+	DC	A(RE68+32)	address of v3 source
00002E40	00002E7C			2381+	DC	A(16)	result length
00002E48	00000000 00000000			2382+REA68	DC	A(RE68)	result address
00002E50	00000000 00000000			2383+	DS	FD	gap
00002E58	00000000 00000000			2384+V1068	DS	XL16	V1 output
00002E60	00000000 00000000						
				2385+	DS	FD	gap
				2386+*			
00002E68				2387+X68	DS	OF	
00002E68	E760 8EAC 0806		000010AC	2388+	VL	V22, V1FUDGE	
00002E6E	E760 0002 2846			2389+	VGM	V22, 0, 2, 2	test instruction (dest is a source)
00002E74	E760 5030 080E		00002E50	2390+	VST	V22, V1068	save v1 output
00002E7A	07FB			2391+	BR	R11	return
00002E7C				2392+RE68	DC	OF	xl16 expected result
00002E7C				2393+	DROP	R5	
00002E7C	E0000000 E0000000			2394	DC	XL16' E0000000E0000000 E0000000E0000000'	result
00002E84	E0000000 E0000000						
				2395			
00002E90				2396	VRI_B	VGM 0, 4, 2	
00002E90		00002E90		2397+	DS	OFD	
00002E90	00002ED8			2398+	USING	*, R5	base for test data and test routine
00002E94	0045			2399+T69	DC	A(X69)	address of test routine
00002E96	00			2400+	DC	H' 69'	test number
00002E97	02			2401+	DC	X' 00'	
00002E98	00			2402+	DC	HL1' 2'	M4 field
00002E98	00			2403+	DC	HL1' 0'	i2 used
00002E99	04			2404+	DC	HL1' 4'	i3 used
00002E9A	E5C7D440 40404040			2405+	DC	CL8' VGM	instruction name
00002EA4	00002EFC			2406+	DC	A(RE69+16)	address of v2 source
00002EA8	00002F0C			2407+	DC	A(RE69+32)	address of v3 source
00002EAC	00000010			2408+	DC	A(16)	result length
00002EB0	00002EEC			2409+REA69	DC	A(RE69)	result address
00002EB8	00000000 00000000			2410+	DS	FD	gap
00002EC0	00000000 00000000			2411+V1069	DS	XL16	V1 output
00002EC8	00000000 00000000						
00002ED0	00000000 00000000			2412+	DS	FD	gap
				2413+*			
00002ED8				2414+X69	DS	OF	
00002ED8	E760 8EAC 0806		000010AC	2415+	VL	V22, V1FUDGE	
00002EDE	E760 0004 2846			2416+	VGM	V22, 0, 4, 2	test instruction (dest is a source)
00002EE4	E760 5030 080E		00002EC0	2417+	VST	V22, V1069	save v1 output
00002EEA	07FB			2418+	BR	R11	return

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00002EEC				2419+RE69	DC	0F	xl16 expected result
00002EEC				2420+	DROP	R5	
00002EEC	F8000000 F8000000			2421	DC	XL16' F8000000F8000000 F8000000F8000000'	result
00002EF4	F8000000 F8000000						
				2422			
				2423	VRI_B	VGM 0, 6, 2	
00002F00				2424+	DS	0FD	
00002F00		00002F00		2425+	USING	*, R5	base for test data and test routine
00002F00	00002F48			2426+T70	DC	A(X70)	address of test routine
00002F04	0046			2427+	DC	H' 70'	test number
00002F06	00			2428+	DC	X' 00'	
00002F07	02			2429+	DC	HL1' 2'	M4 field
00002F08	00			2430+	DC	HL1' 0'	i2 used
00002F09	06			2431+	DC	HL1' 6'	i3 used
00002F0A	E5C7D440 40404040			2432+	DC	CL8' VGM	instruction name
00002F14	00002F6C			2433+	DC	A(RE70+16)	address of v2 source
00002F18	00002F7C			2434+	DC	A(RE70+32)	address of v3 source
00002F1C	00000010			2435+	DC	A(16)	result length
00002F20	00002F5C			2436+REA70	DC	A(RE70)	result address
00002F28	00000000 00000000			2437+	DS	FD	gap
00002F30	00000000 00000000			2438+V1070	DS	XL16	V1 output
00002F38	00000000 00000000						
00002F40	00000000 00000000			2439+	DS	FD	gap
				2440+*			
00002F48				2441+X70	DS	0F	
00002F48	E760 8EAC 0806		000010AC	2442+	VL	V22, V1FUDGE	
00002F4E	E760 0006 2846			2443+	VGM	V22, 0, 6, 2	test instruction (dest is a source)
00002F54	E760 5030 080E		00002F30	2444+	VST	V22, V1070	save v1 output
00002F5A	07FB			2445+	BR	R11	return
00002F5C				2446+RE70	DC	0F	xl16 expected result
00002F5C				2447+	DROP	R5	
00002F5C	FE000000 FE000000			2448	DC	XL16' FE000000FE000000 FE000000FE000000'	result
00002F64	FE000000 FE000000						
				2449			
				2450	VRI_B	VGM 0, 7, 2	
00002F70				2451+	DS	0FD	
00002F70		00002F70		2452+	USING	*, R5	base for test data and test routine
00002F70	00002FB8			2453+T71	DC	A(X71)	address of test routine
00002F74	0047			2454+	DC	H' 71'	test number
00002F76	00			2455+	DC	X' 00'	
00002F77	02			2456+	DC	HL1' 2'	M4 field
00002F78	00			2457+	DC	HL1' 0'	i2 used
00002F79	07			2458+	DC	HL1' 7'	i3 used
00002F7A	E5C7D440 40404040			2459+	DC	CL8' VGM	instruction name
00002F84	00002FDC			2460+	DC	A(RE71+16)	address of v2 source
00002F88	00002FEC			2461+	DC	A(RE71+32)	address of v3 source
00002F8C	00000010			2462+	DC	A(16)	result length
00002F90	00002FCC			2463+REA71	DC	A(RE71)	result address
00002F98	00000000 00000000			2464+	DS	FD	gap
00002FA0	00000000 00000000			2465+V1071	DS	XL16	V1 output
00002FA8	00000000 00000000						
00002FB0	00000000 00000000			2466+	DS	FD	gap
				2467+*			
00002FB8				2468+X71	DS	0F	
00002FB8	E760 8EAC 0806		000010AC	2469+	VL	V22, V1FUDGE	
00002FBE	E760 0007 2846			2470+	VGM	V22, 0, 7, 2	test instruction (dest is a source)



LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00002FC4	E760 5030 080E		00002FA0	2471+	VST	V22, V1071	save v1 output
00002FCA	07FB			2472+	BR	R11	return
00002FCC				2473+RE71	DC	0F	xl16 expected result
00002FCC				2474+	DROP	R5	
00002FCC	FF000000 FF000000			2475	DC	XL16' FF000000FF000000 FF000000FF000000'	result t
00002FD4	FF000000 FF000000						
				2476			
				2477	VRI_B	VGM 0, 8, 2	
00002FE0				2478+	DS	0FD	
00002FE0		00002FE0		2479+	USING	*, R5	base for test data and test routine
00002FE0	00003028			2480+T72	DC	A(X72)	address of test routine
00002FE4	0048			2481+	DC	H' 72'	test number
00002FE6	00			2482+	DC	X' 00'	
00002FE7	02			2483+	DC	HL1' 2'	M4 field
00002FE8	00			2484+	DC	HL1' 0'	i2 used
00002FE9	08			2485+	DC	HL1' 8'	i3 used
00002FEA	E5C7D440 40404040			2486+	DC	CL8' VGM	instruction name
00002FF4	0000304C			2487+	DC	A(RE72+16)	address of v2 source
00002FF8	0000305C			2488+	DC	A(RE72+32)	address of v3 source
00002FFC	00000010			2489+	DC	A(16)	result length
00003000	0000303C			2490+REA72	DC	A(RE72)	result address
00003008	00000000 00000000			2491+	DS	FD	gap
00003010	00000000 00000000			2492+V1072	DS	XL16	V1 output
00003018	00000000 00000000						
00003020	00000000 00000000			2493+	DS	FD	gap
				2494+*			
00003028				2495+X72	DS	0F	
00003028	E760 8EAC 0806		000010AC	2496+	VL	V22, V1FUDGE	
0000302E	E760 0008 2846			2497+	VGM	V22, 0, 8, 2	test instruction (dest is a source)
00003034	E760 5030 080E		00003010	2498+	VST	V22, V1072	save v1 output
0000303A	07FB			2499+	BR	R11	return
0000303C				2500+RE72	DC	0F	xl16 expected result
0000303C				2501+	DROP	R5	
0000303C	FF800000 FF800000			2502	DC	XL16' FF800000FF800000 FF800000FF800000'	result t
00003044	FF800000 FF800000						
				2503			
				2504	VRI_B	VGM 0, 9, 2	
00003050				2505+	DS	0FD	
00003050		00003050		2506+	USING	*, R5	base for test data and test routine
00003050	00003098			2507+T73	DC	A(X73)	address of test routine
00003054	0049			2508+	DC	H' 73'	test number
00003056	00			2509+	DC	X' 00'	
00003057	02			2510+	DC	HL1' 2'	M4 field
00003058	00			2511+	DC	HL1' 0'	i2 used
00003059	09			2512+	DC	HL1' 9'	i3 used
0000305A	E5C7D440 40404040			2513+	DC	CL8' VGM	instruction name
00003064	000030BC			2514+	DC	A(RE73+16)	address of v2 source
00003068	000030CC			2515+	DC	A(RE73+32)	address of v3 source
0000306C	00000010			2516+	DC	A(16)	result length
00003070	000030AC			2517+REA73	DC	A(RE73)	result address
00003078	00000000 00000000			2518+	DS	FD	gap
00003080	00000000 00000000			2519+V1073	DS	XL16	V1 output
00003088	00000000 00000000						
00003090	00000000 00000000			2520+	DS	FD	gap
				2521+*			
00003098				2522+X73	DS	0F	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00003098	E760 8EAC 0806		000010AC	2523+	VL	V22, V1FUDGE	
0000309E	E760 0009 2846			2524+	VGM	V22, 0, 9, 2	test instruction (dest is a source)
000030A4	E760 5030 080E		00003080	2525+	VST	V22, V1073	save v1 output
000030AA	07FB			2526+	BR	R11	return
000030AC				2527+RE73	DC	0F	xl16 expected result
000030AC				2528+	DROP	R5	
000030AC	FFC00000 FFC00000			2529	DC	XL16' FFC00000FFC00000 FFC00000FFC00000'	result
000030B4	FFC00000 FFC00000						
				2530			
000030C0				2531	VRI_B	VGM 0, 11, 2	
000030C0		000030C0		2532+	DS	0FD	
000030C0	00003108			2533+	USING	*, R5	base for test data and test routine
000030C4	004A			2534+T74	DC	A(X74)	address of test routine
000030C6	00			2535+	DC	H' 74'	test number
000030C7	02			2536+	DC	X' 00'	
000030C8	00			2537+	DC	HL1' 2'	M4 field
000030C9	0B			2538+	DC	HL1' 0'	i2 used
000030CA	E5C7D440 40404040			2539+	DC	HL1' 11'	i3 used
000030D4	0000312C			2540+	DC	CL8' VGM	instruction name
000030D8	0000313C			2541+	DC	A(RE74+16)	address of v2 source
000030DC	00000010			2542+	DC	A(RE74+32)	address of v3 source
000030E0	0000311C			2543+	DC	A(16)	result length
000030E8	00000000 00000000			2544+REA74	DC	A(RE74)	result address
000030F0	00000000 00000000			2545+	DS	FD	gap
000030F8	00000000 00000000			2546+V1074	DS	XL16	V1 output
00003100	00000000 00000000			2547+	DS	FD	gap
				2548+*			
00003108				2549+X74	DS	0F	
00003108	E760 8EAC 0806		000010AC	2550+	VL	V22, V1FUDGE	
0000310E	E760 000B 2846			2551+	VGM	V22, 0, 11, 2	test instruction (dest is a source)
00003114	E760 5030 080E		000030F0	2552+	VST	V22, V1074	save v1 output
0000311A	07FB			2553+	BR	R11	return
0000311C				2554+RE74	DC	0F	xl16 expected result
0000311C				2555+	DROP	R5	
0000311C	FFF00000 FFF00000			2556	DC	XL16' FFF00000FFF00000 FFF00000FFF00000'	result
00003124	FFF00000 FFF00000						
				2557			
00003130				2558	VRI_B	VGM 0, 13, 2	
00003130		00003130		2559+	DS	0FD	
00003130	00003178			2560+	USING	*, R5	base for test data and test routine
00003134	004B			2561+T75	DC	A(X75)	address of test routine
00003136	00			2562+	DC	H' 75'	test number
00003137	02			2563+	DC	X' 00'	
00003138	00			2564+	DC	HL1' 2'	M4 field
00003138	00			2565+	DC	HL1' 0'	i2 used
00003139	0D			2566+	DC	HL1' 13'	i3 used
0000313A	E5C7D440 40404040			2567+	DC	CL8' VGM	instruction name
00003144	0000319C			2568+	DC	A(RE75+16)	address of v2 source
00003148	000031AC			2569+	DC	A(RE75+32)	address of v3 source
0000314C	00000010			2570+	DC	A(16)	result length
00003150	0000318C			2571+REA75	DC	A(RE75)	result address
00003158	00000000 00000000			2572+	DS	FD	gap
00003160	00000000 00000000			2573+V1075	DS	XL16	V1 output
00003168	00000000 00000000						
00003170	00000000 00000000			2574+	DS	FD	gap

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00003178				2575+*			
00003178	E760 8EAC 0806		000010AC	2576+X75	DS	0F	
0000317E	E760 000D 2846			2577+	VL	V22, V1FUDGE	
00003184	E760 5030 080E		00003160	2578+	VGM	V22, 0, 13, 2	test instruction (dest is a source)
0000318A	07FB			2579+	VST	V22, V1075	save v1 output
0000318C				2580+	BR	R11	return
0000318C				2581+RE75	DC	0F	xl16 expected result
0000318C	FFFC0000 FFFC0000			2582+	DROP	R5	
00003194	FFFC0000 FFFC0000			2583	DC	XL16' FFFC0000FFFC0000 FFFC0000FFFC0000'	result
000031A0				2584			
000031A0		000031A0		2585	VRI_B	VGM 0, 15, 2	
000031A0	000031E8			2586+	DS	0FD	
000031A4	004C			2587+	USING	*, R5	base for test data and test routine
000031A6	00			2588+T76	DC	A(X76)	address of test routine
000031A7	02			2589+	DC	H' 76'	test number
000031A8	00			2590+	DC	X' 00'	
000031A9	0F			2591+	DC	HL1' 2'	M4 field
000031AA	E5C7D440 40404040			2592+	DC	HL1' 0'	i2 used
000031B4	0000320C			2593+	DC	HL1' 15'	i3 used
000031B8	0000321C			2594+	DC	CL8' VGM	instruction name
000031BC	00000010			2595+	DC	A(RE76+16)	address of v2 source
000031C0	000031FC			2596+	DC	A(RE76+32)	address of v3 source
000031C8	00000000 00000000			2597+	DC	A(16)	result length
000031D0	00000000 00000000			2598+REA76	DC	A(RE76)	result address
000031D8	00000000 00000000			2599+	DS	FD	gap
000031E0	00000000 00000000			2600+V1076	DS	XL16	V1 output
000031E8				2601+	DS	FD	gap
000031E8	E760 8EAC 0806		000010AC	2602+*			
000031EE	E760 000F 2846			2603+X76	DS	0F	
000031F4	E760 5030 080E		000031D0	2604+	VL	V22, V1FUDGE	
000031FA	07FB			2605+	VGM	V22, 0, 15, 2	test instruction (dest is a source)
000031FC				2606+	VST	V22, V1076	save v1 output
000031FC				2607+	BR	R11	return
000031FC	FFFF0000 FFFF0000			2608+RE76	DC	0F	xl16 expected result
00003204	FFFF0000 FFFF0000			2609+	DROP	R5	
00003210				2610	DC	XL16' FFFF0000FFFF0000 FFFF0000FFFF0000'	result
00003210				2611			
00003210		00003210		2612	VRI_B	VGM 0, 16, 2	
00003210	00003258			2613+	DS	0FD	
00003214	004D			2614+	USING	*, R5	base for test data and test routine
00003216	00			2615+T77	DC	A(X77)	address of test routine
00003217	02			2616+	DC	H' 77'	test number
00003218	00			2617+	DC	X' 00'	
00003219	10			2618+	DC	HL1' 2'	M4 field
0000321A	E5C7D440 40404040			2619+	DC	HL1' 0'	i2 used
00003224	0000327C			2620+	DC	HL1' 16'	i3 used
00003228	0000328C			2621+	DC	CL8' VGM	instruction name
0000322C	00000010			2622+	DC	A(RE77+16)	address of v2 source
00003230	0000326C			2623+	DC	A(RE77+32)	address of v3 source
00003238	00000000 00000000			2624+	DC	A(16)	result length
00003240	00000000 00000000			2625+REA77	DC	A(RE77)	result address
				2626+	DS	FD	gap
				2627+V1077	DS	XL16	V1 output

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00003248	00000000 00000000						
00003250	00000000 00000000			2628+	DS	FD	gap
				2629+*			
00003258				2630+X77	DS	OF	
00003258	E760 8EAC 0806		000010AC	2631+	VL	V22, V1FUDGE	
0000325E	E760 0010 2846			2632+	VGM	V22, 0, 16, 2	test instruction (dest is a source)
00003264	E760 5030 080E		00003240	2633+	VST	V22, V1077	save v1 output
0000326A	07FB			2634+	BR	R11	return
0000326C				2635+RE77	DC	OF	xl16 expected result
0000326C				2636+	DROP	R5	
0000326C	FFFF8000 FFFF8000			2637	DC	XL16' FFFF8000FFFF8000 FFFF8000FFFF8000'	result t
00003274	FFFF8000 FFFF8000						
				2638			
				2639	VRI_B	VGM 0, 17, 2	
00003280				2640+	DS	OFD	
00003280		00003280		2641+	USING	*, R5	base for test data and test routine
00003280	000032C8			2642+T78	DC	A(X78)	address of test routine
00003284	004E			2643+	DC	H' 78'	test number
00003286	00			2644+	DC	X' 00'	
00003287	02			2645+	DC	HL1' 2'	M4 field
00003288	00			2646+	DC	HL1' 0'	i2 used
00003289	11			2647+	DC	HL1' 17'	i3 used
0000328A	E5C7D440 40404040			2648+	DC	CL8' VGM	instruction name
00003294	000032EC			2649+	DC	A(RE78+16)	address of v2 source
00003298	000032FC			2650+	DC	A(RE78+32)	address of v3 source
0000329C	00000010			2651+	DC	A(16)	result length
000032A0	000032DC			2652+REA78	DC	A(RE78)	result address
000032A8	00000000 00000000			2653+	DS	FD	gap
000032B0	00000000 00000000			2654+V1078	DS	XL16	V1 output
000032B8	00000000 00000000						
000032C0	00000000 00000000			2655+	DS	FD	gap
				2656+*			
000032C8				2657+X78	DS	OF	
000032C8	E760 8EAC 0806		000010AC	2658+	VL	V22, V1FUDGE	
000032CE	E760 0011 2846			2659+	VGM	V22, 0, 17, 2	test instruction (dest is a source)
000032D4	E760 5030 080E		000032B0	2660+	VST	V22, V1078	save v1 output
000032DA	07FB			2661+	BR	R11	return
000032DC				2662+RE78	DC	OF	xl16 expected result
000032DC				2663+	DROP	R5	
000032DC	FFFFC000 FFFFC000			2664	DC	XL16' FFFFC000FFFC000 FFFFC000FFFC000'	result t
000032E4	FFFC000 FFFFC000						
				2665			
				2666	VRI_B	VGM 0, 25, 2	
000032F0				2667+	DS	OFD	
000032F0		000032F0		2668+	USING	*, R5	base for test data and test routine
000032F0	00003338			2669+T79	DC	A(X79)	address of test routine
000032F4	004F			2670+	DC	H' 79'	test number
000032F6	00			2671+	DC	X' 00'	
000032F7	02			2672+	DC	HL1' 2'	M4 field
000032F8	00			2673+	DC	HL1' 0'	i2 used
000032F9	19			2674+	DC	HL1' 25'	i3 used
000032FA	E5C7D440 40404040			2675+	DC	CL8' VGM	instruction name
00003304	0000335C			2676+	DC	A(RE79+16)	address of v2 source
00003308	0000336C			2677+	DC	A(RE79+32)	address of v3 source
0000330C	00000010			2678+	DC	A(16)	result length
00003310	0000334C			2679+REA79	DC	A(RE79)	result address



LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00003318	00000000 00000000			2680+	DS	FD	gap
00003320	00000000 00000000			2681+V1079	DS	XL16	V1 output
00003328	00000000 00000000						
00003330	00000000 00000000			2682+	DS	FD	gap
				2683+*			
00003338				2684+X79	DS	OF	
00003338	E760 8EAC 0806		000010AC	2685+	VL	V22, V1FUDGE	
0000333E	E760 0019 2846			2686+	VGM	V22, 0, 25, 2	test instruction (dest is a source)
00003344	E760 5030 080E		00003320	2687+	VST	V22, V1079	save v1 output
0000334A	07FB			2688+	BR	R11	return
0000334C				2689+RE79	DC	OF	xl16 expected result
0000334C				2690+	DROP	R5	
0000334C	FFFFFFFFC0 FFFFFFFC0			2691	DC	XL16' FFFFFFFC0FFFFFFC0 FFFFFFFC0FFFFFFC0'	result
00003354	FFFFFFFFC0 FFFFFFFC0						
				2692			
				2693	VRI_B	VGM 0, 30, 2	
00003360				2694+	DS	OFD	
00003360		00003360		2695+	USING	*, R5	base for test data and test routine
00003360	000033A8			2696+T80	DC	A(X80)	address of test routine
00003364	0050			2697+	DC	H' 80'	test number
00003366	00			2698+	DC	X' 00'	
00003367	02			2699+	DC	HL1' 2'	M4 field
00003368	00			2700+	DC	HL1' 0'	i2 used
00003369	1E			2701+	DC	HL1' 30'	i3 used
0000336A	E5C7D440 40404040			2702+	DC	CL8' VGM	instruction name
00003374	000033CC			2703+	DC	A(RE80+16)	address of v2 source
00003378	000033DC			2704+	DC	A(RE80+32)	address of v3 source
0000337C	00000010			2705+	DC	A(16)	result length
00003380	000033BC			2706+REA80	DC	A(RE80)	result address
00003388	00000000 00000000			2707+	DS	FD	gap
00003390	00000000 00000000			2708+V1080	DS	XL16	V1 output
00003398	00000000 00000000						
000033A0	00000000 00000000			2709+	DS	FD	gap
				2710+*			
000033A8				2711+X80	DS	OF	
000033A8	E760 8EAC 0806		000010AC	2712+	VL	V22, V1FUDGE	
000033AE	E760 001E 2846			2713+	VGM	V22, 0, 30, 2	test instruction (dest is a source)
000033B4	E760 5030 080E		00003390	2714+	VST	V22, V1080	save v1 output
000033BA	07FB			2715+	BR	R11	return
000033BC				2716+RE80	DC	OF	xl16 expected result
000033BC				2717+	DROP	R5	
000033BC	FFFFFFFFFE FFFFFFFFE			2718	DC	XL16' FFFFFFFFEFFFFFFFE FFFFFFFFEFFFFFFFE'	result
000033C4	FFFFFFFFFE FFFFFFFFE						
				2719			
				2720	VRI_B	VGM 0, 31, 2	
000033D0				2721+	DS	OFD	
000033D0		000033D0		2722+	USING	*, R5	base for test data and test routine
000033D0	00003418			2723+T81	DC	A(X81)	address of test routine
000033D4	0051			2724+	DC	H' 81'	test number
000033D6	00			2725+	DC	X' 00'	
000033D7	02			2726+	DC	HL1' 2'	M4 field
000033D8	00			2727+	DC	HL1' 0'	i2 used
000033D9	1F			2728+	DC	HL1' 31'	i3 used
000033DA	E5C7D440 40404040			2729+	DC	CL8' VGM	instruction name
000033E4	0000343C			2730+	DC	A(RE81+16)	address of v2 source
000033E8	0000344C			2731+	DC	A(RE81+32)	address of v3 source



LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
000033EC	00000010			2732+	DC	A(16)	result length
000033F0	0000342C			2733+REA81	DC	A(RE81)	result address
000033F8	00000000 00000000			2734+	DS	FD	gap
00003400	00000000 00000000			2735+V1081	DS	XL16	V1 output
00003408	00000000 00000000						
00003410	00000000 00000000			2736+	DS	FD	gap
				2737+*			
00003418				2738+X81	DS	OF	
00003418	E760 8EAC 0806		000010AC	2739+	VL	V22, V1FUDGE	
0000341E	E760 001F 2846			2740+	VGM	V22, 0, 31, 2	test instruction (dest is a source)
00003424	E760 5030 080E		00003400	2741+	VST	V22, V1081	save v1 output
0000342A	07FB			2742+	BR	R11	return
0000342C				2743+RE81	DC	OF	xl16 expected result
0000342C				2744+	DROP	R5	
0000342C	FFFFFFFF FFFFFFFF			2745	DC	XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF'	result
00003434	FFFFFFFF FFFFFFFF						
				2746			
00003440				2747	VRI_B	VGM 0, 32, 2	
00003440		00003440		2748+	DS	OFD	
00003440	00003488			2749+	USING	*, R5	base for test data and test routine
00003444	0052			2750+T82	DC	A(X82)	address of test routine
00003446	00			2751+	DC	H' 82'	test number
00003447	02			2752+	DC	X' 00'	
00003448	00			2753+	DC	HL1' 2'	M4 field
00003448	00			2754+	DC	HL1' 0'	i2 used
00003449	20			2755+	DC	HL1' 32'	i3 used
0000344A	E5C7D440 40404040			2756+	DC	CL8' VGM	instruction name
00003454	000034AC			2757+	DC	A(RE82+16)	address of v2 source
00003458	000034BC			2758+	DC	A(RE82+32)	address of v3 source
0000345C	00000010			2759+	DC	A(16)	result length
00003460	0000349C			2760+REA82	DC	A(RE82)	result address
00003468	00000000 00000000			2761+	DS	FD	gap
00003470	00000000 00000000			2762+V1082	DS	XL16	V1 output
00003478	00000000 00000000						
00003480	00000000 00000000			2763+	DS	FD	gap
				2764+*			
00003488				2765+X82	DS	OF	
00003488	E760 8EAC 0806		000010AC	2766+	VL	V22, V1FUDGE	
0000348E	E760 0020 2846			2767+	VGM	V22, 0, 32, 2	test instruction (dest is a source)
00003494	E760 5030 080E		00003470	2768+	VST	V22, V1082	save v1 output
0000349A	07FB			2769+	BR	R11	return
0000349C				2770+RE82	DC	OF	xl16 expected result
0000349C				2771+	DROP	R5	
0000349C	80000000 80000000			2772	DC	XL16' 8000000080000000 8000000080000000'	result
000034A4	80000000 80000000						
				2773			
000034B0				2774	VRI_B	VGM 0, 64, 2	
000034B0		000034B0		2775+	DS	OFD	
000034B0	000034F8			2776+	USING	*, R5	base for test data and test routine
000034B4	0053			2777+T83	DC	A(X83)	address of test routine
000034B6	00			2778+	DC	H' 83'	test number
000034B7	02			2779+	DC	X' 00'	
000034B8	00			2780+	DC	HL1' 2'	M4 field
000034B8	00			2781+	DC	HL1' 0'	i2 used
000034B9	40			2782+	DC	HL1' 64'	i3 used
000034BA	E5C7D440 40404040			2783+	DC	CL8' VGM	instruction name



LOC	OBJECT CODE	ADDR1	ADDR2	STMT	
				2802 *Word: I2<I3; I2=1	
				2803 VRI_B VGM 1, 1, 2	
00003520				2804+ DS OFD	
00003520		00003520		2805+ USING *, R5	base for test data and test routine
00003520	00003568			2806+T84 DC A(X84)	address of test routine
00003524	0054			2807+ DC H' 84'	test number
00003526	00			2808+ DC X' 00'	
00003527	02			2809+ DC HL1' 2'	M4 field
00003528	01			2810+ DC HL1' 1'	i2 used
00003529	01			2811+ DC HL1' 1'	i3 used
0000352A	E5C7D440 40404040			2812+ DC CL8' VGM	instruction name
00003534	0000358C			2813+ DC A(RE84+16)	address of v2 source
00003538	0000359C			2814+ DC A(RE84+32)	address of v3 source
0000353C	00000010			2815+ DC A(16)	result length
00003540	0000357C			2816+REA84 DC A(RE84)	result address
00003548	00000000 00000000			2817+ DS FD	gap
00003550	00000000 00000000			2818+V1084 DS XL16	V1 output
00003558	00000000 00000000				
00003560	00000000 00000000			2819+ DS FD	gap
				2820+*	
00003568				2821+X84 DS OF	
00003568	E760 8EAC 0806		000010AC	2822+ VL V22, V1FUDGE	
0000356E	E760 0101 2846			2823+ VGM V22, 1, 1, 2	test instruction (dest is a source)
00003574	E760 5030 080E		00003550	2824+ VST V22, V1084	save v1 output
0000357A	07FB			2825+ BR R11	return
0000357C				2826+RE84 DC OF	xl16 expected result
0000357C				2827+ DROP R5	
0000357C	40000000 40000000			2828 DC XL16' 4000000040000000 4000000040000000'	result t
00003584	40000000 40000000				
				2829	
				2830 VRI_B VGM 1, 2, 2	
00003590				2831+ DS OFD	
00003590		00003590		2832+ USING *, R5	base for test data and test routine
00003590	000035D8			2833+T85 DC A(X85)	address of test routine
00003594	0055			2834+ DC H' 85'	test number
00003596	00			2835+ DC X' 00'	
00003597	02			2836+ DC HL1' 2'	M4 field
00003598	01			2837+ DC HL1' 1'	i2 used
00003599	02			2838+ DC HL1' 2'	i3 used
0000359A	E5C7D440 40404040			2839+ DC CL8' VGM	instruction name
000035A4	000035FC			2840+ DC A(RE85+16)	address of v2 source
000035A8	0000360C			2841+ DC A(RE85+32)	address of v3 source
000035AC	00000010			2842+ DC A(16)	result length
000035B0	000035EC			2843+REA85 DC A(RE85)	result address
000035B8	00000000 00000000			2844+ DS FD	gap
000035C0	00000000 00000000			2845+V1085 DS XL16	V1 output
000035C8	00000000 00000000				
000035D0	00000000 00000000			2846+ DS FD	gap
				2847+*	
000035D8				2848+X85 DS OF	
000035D8	E760 8EAC 0806		000010AC	2849+ VL V22, V1FUDGE	
000035DE	E760 0102 2846			2850+ VGM V22, 1, 2, 2	test instruction (dest is a source)
000035E4	E760 5030 080E		000035C0	2851+ VST V22, V1085	save v1 output
000035EA	07FB			2852+ BR R11	return
000035EC				2853+RE85 DC OF	xl16 expected result
000035EC				2854+ DROP R5	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT				
000035EC	60000000 60000000			2855	DC	XL16' 60000000060000000 6000000060000000'	result	
000035F4	60000000 60000000							
				2856				
00003600				2857	VRI_B	VGM 1, 4, 2		
00003600		00003600		2858+	DS	OFD		
00003600	00003648			2859+	USING	*, R5	base for test data and test routine	
00003604	0056			2860+T86	DC	A(X86)	address of test routine	
00003606	00			2861+	DC	H' 86'	test number	
00003607	02			2862+	DC	X' 00'		
00003608	01			2863+	DC	HL1' 2'	M4 field	
00003609	04			2864+	DC	HL1' 1'	i2 used	
0000360A	E5C7D440 40404040			2865+	DC	HL1' 4'	i3 used	
00003614	0000366C			2866+	DC	CL8' VGM	instruction name	
00003618	0000367C			2867+	DC	A(RE86+16)	address of v2 source	
0000361C	00000010			2868+	DC	A(RE86+32)	address of v3 source	
00003620	0000365C			2869+	DC	A(16)	result length	
00003628	00000000 00000000			2870+REA86	DC	A(RE86)	result address	
00003630	00000000 00000000			2871+	DS	FD	gap	
00003638	00000000 00000000			2872+V1086	DS	XL16	V1 output	
00003640	00000000 00000000							
				2873+	DS	FD	gap	
				2874+*				
00003648				2875+X86	DS	OF		
00003648	E760 8EAC 0806		000010AC	2876+	VL	V22, V1FUDGE		
0000364E	E760 0104 2846			2877+	VGM	V22, 1, 4, 2	test instruction (dest is a source)	
00003654	E760 5030 080E		00003630	2878+	VST	V22, V1086	save v1 output	
0000365A	07FB			2879+	BR	R11	return	
0000365C				2880+RE86	DC	OF	xl16 expected result	
0000365C				2881+	DROP	R5		
0000365C	78000000 78000000			2882	DC	XL16' 78000000078000000 7800000078000000'	result	
00003664	78000000 78000000							
				2883				
00003670				2884	VRI_B	VGM 1, 6, 2		
00003670		00003670		2885+	DS	OFD		
00003670	000036B8			2886+	USING	*, R5	base for test data and test routine	
00003674	0057			2887+T87	DC	A(X87)	address of test routine	
00003676	00			2888+	DC	H' 87'	test number	
00003677	00			2889+	DC	X' 00'		
00003677	02			2890+	DC	HL1' 2'	M4 field	
00003678	01			2891+	DC	HL1' 1'	i2 used	
00003679	06			2892+	DC	HL1' 6'	i3 used	
0000367A	E5C7D440 40404040			2893+	DC	CL8' VGM	instruction name	
00003684	000036DC			2894+	DC	A(RE87+16)	address of v2 source	
00003688	000036EC			2895+	DC	A(RE87+32)	address of v3 source	
0000368C	00000010			2896+	DC	A(16)	result length	
00003690	000036CC			2897+REA87	DC	A(RE87)	result address	
00003698	00000000 00000000			2898+	DS	FD	gap	
000036A0	00000000 00000000			2899+V1087	DS	XL16	V1 output	
000036A8	00000000 00000000							
000036B0	00000000 00000000			2900+	DS	FD	gap	
				2901+*				
000036B8				2902+X87	DS	OF		
000036B8	E760 8EAC 0806		000010AC	2903+	VL	V22, V1FUDGE		
000036BE	E760 0106 2846			2904+	VGM	V22, 1, 6, 2	test instruction (dest is a source)	
000036C4	E760 5030 080E		000036A0	2905+	VST	V22, V1087	save v1 output	
000036CA	07FB			2906+	BR	R11	return	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
000036CC				2907+RE87	DC	0F	xl16 expected result
000036CC				2908+	DROP	R5	
000036CC	7E000000 7E000000			2909	DC	XL16' 7E00000007E000000 7E0000007E000000'	result
000036D4	7E000000 7E000000						
				2910			
000036E0				2911	VRI_B	VGM 1, 7, 2	
000036E0		000036E0		2912+	DS	0FD	
000036E0	00003728			2913+	USING	*, R5	base for test data and test routine
000036E4	0058			2914+T88	DC	A(X88)	address of test routine
000036E6	00			2915+	DC	H' 88'	test number
000036E7	02			2916+	DC	X' 00'	
000036E8	01			2917+	DC	HL1' 2'	M4 field
000036E9	07			2918+	DC	HL1' 1'	i2 used
000036EA	E5C7D440 40404040			2919+	DC	HL1' 7'	i3 used
000036F4	0000374C			2920+	DC	CL8' VGM	instruction name
000036F8	0000375C			2921+	DC	A(RE88+16)	address of v2 source
000036FC	00000010			2922+	DC	A(RE88+32)	address of v3 source
00003700	0000373C			2923+	DC	A(16)	result length
00003708	00000000 00000000			2924+REA88	DC	A(RE88)	result address
00003710	00000000 00000000			2925+	DS	FD	gap
00003718	00000000 00000000			2926+V1088	DS	XL16	V1 output
00003720	00000000 00000000			2927+	DS	FD	gap
				2928+*			
00003728				2929+X88	DS	0F	
00003728	E760 8EAC 0806		000010AC	2930+	VL	V22, V1FUDGE	
0000372E	E760 0107 2846			2931+	VGM	V22, 1, 7, 2	test instruction (dest is a source)
00003734	E760 5030 080E		00003710	2932+	VST	V22, V1088	save v1 output
0000373A	07FB			2933+	BR	R11	return
0000373C				2934+RE88	DC	0F	xl16 expected result
0000373C				2935+	DROP	R5	
0000373C	7F000000 7F000000			2936	DC	XL16' 7F00000007F000000 7F0000007F000000'	result
00003744	7F000000 7F000000						
				2937			
00003750				2938	VRI_B	VGM 1, 8, 2	
00003750		00003750		2939+	DS	0FD	
00003750	00003798			2940+	USING	*, R5	base for test data and test routine
00003754	0059			2941+T89	DC	A(X89)	address of test routine
00003756	00			2942+	DC	H' 89'	test number
00003757	02			2943+	DC	X' 00'	
00003758	01			2944+	DC	HL1' 2'	M4 field
00003759	08			2945+	DC	HL1' 1'	i2 used
0000375A	E5C7D440 40404040			2946+	DC	HL1' 8'	i3 used
00003764	000037BC			2947+	DC	CL8' VGM	instruction name
00003768	000037CC			2948+	DC	A(RE89+16)	address of v2 source
0000376C	00000010			2949+	DC	A(RE89+32)	address of v3 source
00003770	000037AC			2950+	DC	A(16)	result length
00003778	00000000 00000000			2951+REA89	DC	A(RE89)	result address
00003780	00000000 00000000			2952+	DS	FD	gap
00003788	00000000 00000000			2953+V1089	DS	XL16	V1 output
00003790	00000000 00000000			2954+	DS	FD	gap
				2955+*			
00003798				2956+X89	DS	0F	
00003798	E760 8EAC 0806		000010AC	2957+	VL	V22, V1FUDGE	
0000379E	E760 0108 2846			2958+	VGM	V22, 1, 8, 2	test instruction (dest is a source)



LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
000037A4	E760 5030 080E		00003780	2959+	VST	V22, V1089	save v1 output
000037AA	07FB			2960+	BR	R11	return
000037AC				2961+RE89	DC	0F	xl16 expected result
000037AC				2962+	DROP	R5	
000037AC	7F800000 7F800000			2963	DC	XL16' 7F8000007F800000 7F8000007F800000'	result t
000037B4	7F800000 7F800000						
				2964			
				2965	VRI_B	VGM 1, 9, 2	
000037C0				2966+	DS	0FD	
000037C0		000037C0		2967+	USING	*, R5	base for test data and test routine
000037C0	00003808			2968+T90	DC	A(X90)	address of test routine
000037C4	005A			2969+	DC	H' 90'	test number
000037C6	00			2970+	DC	X' 00'	
000037C7	02			2971+	DC	HL1' 2'	M4 field
000037C8	01			2972+	DC	HL1' 1'	i2 used
000037C9	09			2973+	DC	HL1' 9'	i3 used
000037CA	E5C7D440 40404040			2974+	DC	CL8' VGM	instruction name
000037D4	0000382C			2975+	DC	A(RE90+16)	address of v2 source
000037D8	0000383C			2976+	DC	A(RE90+32)	address of v3 source
000037DC	00000010			2977+	DC	A(16)	result length
000037E0	0000381C			2978+REA90	DC	A(RE90)	result address
000037E8	00000000 00000000			2979+	DS	FD	gap
000037F0	00000000 00000000			2980+V1090	DS	XL16	V1 output
000037F8	00000000 00000000						
00003800	00000000 00000000			2981+	DS	FD	gap
				2982+*			
00003808				2983+X90	DS	0F	
00003808	E760 8EAC 0806		000010AC	2984+	VL	V22, V1FUDGE	
0000380E	E760 0109 2846			2985+	VGM	V22, 1, 9, 2	test instruction (dest is a source)
00003814	E760 5030 080E		000037F0	2986+	VST	V22, V1090	save v1 output
0000381A	07FB			2987+	BR	R11	return
0000381C				2988+RE90	DC	0F	xl16 expected result
0000381C				2989+	DROP	R5	
0000381C	7FC00000 7FC00000			2990	DC	XL16' 7FC000007FC00000 7FC000007FC00000'	result t
00003824	7FC00000 7FC00000						
				2991			
				2992	VRI_B	VGM 1, 11, 2	
00003830				2993+	DS	0FD	
00003830		00003830		2994+	USING	*, R5	base for test data and test routine
00003830	00003878			2995+T91	DC	A(X91)	address of test routine
00003834	005B			2996+	DC	H' 91'	test number
00003836	00			2997+	DC	X' 00'	
00003837	02			2998+	DC	HL1' 2'	M4 field
00003838	01			2999+	DC	HL1' 1'	i2 used
00003839	0B			3000+	DC	HL1' 11'	i3 used
0000383A	E5C7D440 40404040			3001+	DC	CL8' VGM	instruction name
00003844	0000389C			3002+	DC	A(RE91+16)	address of v2 source
00003848	000038AC			3003+	DC	A(RE91+32)	address of v3 source
0000384C	00000010			3004+	DC	A(16)	result length
00003850	0000388C			3005+REA91	DC	A(RE91)	result address
00003858	00000000 00000000			3006+	DS	FD	gap
00003860	00000000 00000000			3007+V1091	DS	XL16	V1 output
00003868	00000000 00000000						
00003870	00000000 00000000			3008+	DS	FD	gap
				3009+*			
00003878				3010+X91	DS	0F	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00003878	E760 8EAC 0806		000010AC	3011+	VL	V22, V1FUDGE	
0000387E	E760 010B 2846			3012+	VGM	V22, 1, 11, 2	test instruction (dest is a source)
00003884	E760 5030 080E		00003860	3013+	VST	V22, V1091	save v1 output
0000388A	07FB			3014+	BR	R11	return
0000388C				3015+RE91	DC	0F	xl16 expected result
0000388C				3016+	DROP	R5	
0000388C	7FF00000 7FF00000			3017	DC	XL16' 7FF000007FF00000 7FF000007FF00000'	result
00003894	7FF00000 7FF00000						
				3018			
				3019	VRI_B	VGM 1, 13, 2	
000038A0				3020+	DS	0FD	
000038A0		000038A0		3021+	USING	*, R5	base for test data and test routine
000038A0	000038E8			3022+T92	DC	A(X92)	address of test routine
000038A4	005C			3023+	DC	H' 92'	test number
000038A6	00			3024+	DC	X' 00'	
000038A7	02			3025+	DC	HL1' 2'	M4 field
000038A8	01			3026+	DC	HL1' 1'	i2 used
000038A9	0D			3027+	DC	HL1' 13'	i3 used
000038AA	E5C7D440 40404040			3028+	DC	CL8' VGM	instruction name
000038B4	0000390C			3029+	DC	A(RE92+16)	address of v2 source
000038B8	0000391C			3030+	DC	A(RE92+32)	address of v3 source
000038BC	00000010			3031+	DC	A(16)	result length
000038C0	000038FC			3032+REA92	DC	A(RE92)	result address
000038C8	00000000 00000000			3033+	DS	FD	gap
000038D0	00000000 00000000			3034+V1092	DS	XL16	V1 output
000038D8	00000000 00000000						
000038E0	00000000 00000000			3035+	DS	FD	gap
				3036+*			
000038E8				3037+X92	DS	0F	
000038E8	E760 8EAC 0806		000010AC	3038+	VL	V22, V1FUDGE	
000038EE	E760 010D 2846			3039+	VGM	V22, 1, 13, 2	test instruction (dest is a source)
000038F4	E760 5030 080E		000038D0	3040+	VST	V22, V1092	save v1 output
000038FA	07FB			3041+	BR	R11	return
000038FC				3042+RE92	DC	0F	xl16 expected result
000038FC				3043+	DROP	R5	
000038FC	7FFC0000 7FFC0000			3044	DC	XL16' 7FFC00007FFC0000 7FFC00007FFC0000'	result
00003904	7FFC0000 7FFC0000						
				3045			
				3046	VRI_B	VGM 1, 15, 2	
00003910				3047+	DS	0FD	
00003910		00003910		3048+	USING	*, R5	base for test data and test routine
00003910	00003958			3049+T93	DC	A(X93)	address of test routine
00003914	005D			3050+	DC	H' 93'	test number
00003916	00			3051+	DC	X' 00'	
00003917	02			3052+	DC	HL1' 2'	M4 field
00003918	01			3053+	DC	HL1' 1'	i2 used
00003919	0F			3054+	DC	HL1' 15'	i3 used
0000391A	E5C7D440 40404040			3055+	DC	CL8' VGM	instruction name
00003924	0000397C			3056+	DC	A(RE93+16)	address of v2 source
00003928	0000398C			3057+	DC	A(RE93+32)	address of v3 source
0000392C	00000010			3058+	DC	A(16)	result length
00003930	0000396C			3059+REA93	DC	A(RE93)	result address
00003938	00000000 00000000			3060+	DS	FD	gap
00003940	00000000 00000000			3061+V1093	DS	XL16	V1 output
00003948	00000000 00000000						
00003950	00000000 00000000			3062+	DS	FD	gap

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00003958				3063+*			
00003958	E760 8EAC 0806		000010AC	3064+X93	DS	0F	
0000395E	E760 010F 2846			3065+	VL	V22, V1FUDGE	
00003964	E760 5030 080E		00003940	3066+	VGM	V22, 1, 15, 2	test instruction (dest is a source)
0000396A	07FB			3067+	VST	V22, V1093	save v1 output
0000396C				3068+	BR	R11	return
0000396C				3069+RE93	DC	0F	xl16 expected result
0000396C	7FFF0000 7FFF0000			3070+	DROP	R5	
00003974	7FFF0000 7FFF0000			3071	DC	XL16' 7FFF00007FFF0000 7FFF00007FFF0000'	result t
				3072			
00003980				3073	VRI_B	VGM, 1, 16, 2	
00003980		00003980		3074+	DS	0FD	
00003980	000039C8			3075+	USING	*, R5	base for test data and test routine
00003984	005E			3076+T94	DC	A(X94)	address of test routine
00003986	00			3077+	DC	H' 94'	test number
00003987	02			3078+	DC	X' 00'	
00003988	01			3079+	DC	HL1' 2'	M4 field
00003989	10			3080+	DC	HL1' 1'	i2 used
0000398A	E5C7D440 40404040			3081+	DC	HL1' 16'	i3 used
00003994	000039EC			3082+	DC	CL8' VGM	instruction name
00003998	000039FC			3083+	DC	A(RE94+16)	address of v2 source
0000399C	00000010			3084+	DC	A(RE94+32)	address of v3 source
000039A0	000039DC			3085+	DC	A(16)	result length
000039A8	00000000 00000000			3086+REA94	DC	A(RE94)	result address
000039B0	00000000 00000000			3087+	DS	FD	gap
000039B8	00000000 00000000			3088+V1094	DS	XL16	V1 output
000039C0	00000000 00000000			3089+	DS	FD	gap
				3090+*			
000039C8				3091+X94	DS	0F	
000039C8	E760 8EAC 0806		000010AC	3092+	VL	V22, V1FUDGE	
000039CE	E760 0110 2846			3093+	VGM	V22, 1, 16, 2	test instruction (dest is a source)
000039D4	E760 5030 080E		000039B0	3094+	VST	V22, V1094	save v1 output
000039DA	07FB			3095+	BR	R11	return
000039DC				3096+RE94	DC	0F	xl16 expected result
000039DC				3097+	DROP	R5	
000039DC	7FFF8000 7FFF8000			3098	DC	XL16' 7FFF80007FFF8000 7FFF80007FFF8000'	result t
000039E4	7FFF8000 7FFF8000						
				3099			
000039F0				3100	VRI_B	VGM, 1, 17, 2	
000039F0		000039F0		3101+	DS	0FD	
000039F0	00003A38			3102+	USING	*, R5	base for test data and test routine
000039F4	005F			3103+T95	DC	A(X95)	address of test routine
000039F6	00			3104+	DC	H' 95'	test number
000039F7	02			3105+	DC	X' 00'	
000039F8	01			3106+	DC	HL1' 2'	M4 field
000039F9	11			3107+	DC	HL1' 1'	i2 used
000039FA	E5C7D440 40404040			3108+	DC	HL1' 17'	i3 used
00003A04	00003A5C			3109+	DC	CL8' VGM	instruction name
00003A08	00003A6C			3110+	DC	A(RE95+16)	address of v2 source
00003A0C	00000010			3111+	DC	A(RE95+32)	address of v3 source
00003A10	00003A4C			3112+	DC	A(16)	result length
00003A18	00000000 00000000			3113+REA95	DC	A(RE95)	result address
00003A20	00000000 00000000			3114+	DS	FD	gap
				3115+V1095	DS	XL16	V1 output

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00003A28	00000000 00000000						
00003A30	00000000 00000000			3116+	DS	FD	gap
				3117+*			
00003A38				3118+X95	DS	0F	
00003A38	E760 8EAC 0806		000010AC	3119+	VL	V22, V1FUDGE	
00003A3E	E760 0111 2846			3120+	VGM	V22, 1, 17, 2	test instruction (dest is a source)
00003A44	E760 5030 080E		00003A20	3121+	VST	V22, V1095	save v1 output
00003A4A	07FB			3122+	BR	R11	return
00003A4C				3123+RE95	DC	0F	xl16 expected result
00003A4C				3124+	DROP	R5	
00003A4C	7FFFC000 7FFFC000			3125	DC	XL16' 7FFFC0007FFFC000 7FFFC0007FFFC000'	result t
00003A54	7FFFC000 7FFFC000						
				3126			
				3127	VRI_B	VGM 1, 25, 2	
00003A60				3128+	DS	0FD	
00003A60		00003A60		3129+	USING	*, R5	base for test data and test routine
00003A60	00003AA8			3130+T96	DC	A(X96)	address of test routine
00003A64	0060			3131+	DC	H' 96'	test number
00003A66	00			3132+	DC	X' 00'	
00003A67	02			3133+	DC	HL1' 2'	M4 field
00003A68	01			3134+	DC	HL1' 1'	i2 used
00003A69	19			3135+	DC	HL1' 25'	i3 used
00003A6A	E5C7D440 40404040			3136+	DC	CL8' VGM	instruction name
00003A74	00003ACC			3137+	DC	A(RE96+16)	address of v2 source
00003A78	00003ADC			3138+	DC	A(RE96+32)	address of v3 source
00003A7C	00000010			3139+	DC	A(16)	result length
00003A80	00003ABC			3140+REA96	DC	A(RE96)	result address
00003A88	00000000 00000000			3141+	DS	FD	gap
00003A90	00000000 00000000			3142+V1096	DS	XL16	V1 output
00003A98	00000000 00000000						
00003AA0	00000000 00000000			3143+	DS	FD	gap
				3144+*			
00003AA8				3145+X96	DS	0F	
00003AA8	E760 8EAC 0806		000010AC	3146+	VL	V22, V1FUDGE	
00003AAE	E760 0119 2846			3147+	VGM	V22, 1, 25, 2	test instruction (dest is a source)
00003AB4	E760 5030 080E		00003A90	3148+	VST	V22, V1096	save v1 output
00003ABA	07FB			3149+	BR	R11	return
00003ABC				3150+RE96	DC	0F	xl16 expected result
00003ABC				3151+	DROP	R5	
00003ABC	7FFFFFFC0 7FFFFFFC0			3152	DC	XL16' 7FFFFFFC07FFFFFFC0 7FFFFFFC07FFFFFFC0'	result t
00003AC4	7FFFFFFC0 7FFFFFFC0						
				3153			
				3154	VRI_B	VGM 1, 30, 2	
00003AD0				3155+	DS	0FD	
00003AD0		00003AD0		3156+	USING	*, R5	base for test data and test routine
00003AD0	00003B18			3157+T97	DC	A(X97)	address of test routine
00003AD4	0061			3158+	DC	H' 97'	test number
00003AD6	00			3159+	DC	X' 00'	
00003AD7	02			3160+	DC	HL1' 2'	M4 field
00003AD8	01			3161+	DC	HL1' 1'	i2 used
00003AD9	1E			3162+	DC	HL1' 30'	i3 used
00003ADA	E5C7D440 40404040			3163+	DC	CL8' VGM	instruction name
00003AE4	00003B3C			3164+	DC	A(RE97+16)	address of v2 source
00003AE8	00003B4C			3165+	DC	A(RE97+32)	address of v3 source
00003AEC	00000010			3166+	DC	A(16)	result length
00003AF0	00003B2C			3167+REA97	DC	A(RE97)	result address







LOC	OBJECT CODE	ADDR1	ADDR2	STMT	
				3209 *Word: I2>I3; I2=0	
				3210 VRI_B VGM 1, 0, 2	
00003BB0				3211+ DS OFD	
00003BB0		00003BB0		3212+ USING *, R5	base for test data and test routine
00003BB0	00003BF8			3213+T99 DC A(X99)	address of test routine
00003BB4	0063			3214+ DC H' 99'	test number
00003BB6	00			3215+ DC X' 00'	
00003BB7	02			3216+ DC HL1' 2'	M4 field
00003BB8	01			3217+ DC HL1' 1'	i2 used
00003BB9	00			3218+ DC HL1' 0'	i3 used
00003BBA	E5C7D440 40404040			3219+ DC CL8' VGM	instruction name
00003BC4	00003C1C			3220+ DC A(RE99+16)	address of v2 source
00003BC8	00003C2C			3221+ DC A(RE99+32)	address of v3 source
00003BCC	00000010			3222+ DC A(16)	result length
00003BD0	00003C0C			3223+REA99 DC A(RE99)	result address
00003BD8	00000000 00000000			3224+ DS FD	gap
00003BE0	00000000 00000000			3225+V1099 DS XL16	V1 output
00003BE8	00000000 00000000				
00003BF0	00000000 00000000			3226+ DS FD	gap
				3227+*	
00003BF8				3228+X99 DS OF	
00003BF8	E760 8EAC 0806	000010AC		3229+ VL V22, V1FUDGE	
00003BFE	E760 0100 2846			3230+ VGM V22, 1, 0, 2	test instruction (dest is a source)
00003C04	E760 5030 080E	00003BE0		3231+ VST V22, V1099	save v1 output
00003C0A	07FB			3232+ BR R11	return
00003C0C				3233+RE99 DC OF	xl16 expected result
00003C0C				3234+ DROP R5	
00003C0C	FFFFFFFF FFFFFFFF			3235 DC XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF'	result t
00003C14	FFFFFFFF FFFFFFFF				
				3236	
				3237 VRI_B VGM 2, 0, 2	
00003C20				3238+ DS OFD	
00003C20		00003C20		3239+ USING *, R5	base for test data and test routine
00003C20	00003C68			3240+T100 DC A(X100)	address of test routine
00003C24	0064			3241+ DC H' 100'	test number
00003C26	00			3242+ DC X' 00'	
00003C27	02			3243+ DC HL1' 2'	M4 field
00003C28	02			3244+ DC HL1' 2'	i2 used
00003C29	00			3245+ DC HL1' 0'	i3 used
00003C2A	E5C7D440 40404040			3246+ DC CL8' VGM	instruction name
00003C34	00003C8C			3247+ DC A(RE100+16)	address of v2 source
00003C38	00003C9C			3248+ DC A(RE100+32)	address of v3 source
00003C3C	00000010			3249+ DC A(16)	result length
00003C40	00003C7C			3250+REA100 DC A(RE100)	result address
00003C48	00000000 00000000			3251+ DS FD	gap
00003C50	00000000 00000000			3252+V10100 DS XL16	V1 output
00003C58	00000000 00000000				
00003C60	00000000 00000000			3253+ DS FD	gap
				3254+*	
00003C68				3255+X100 DS OF	
00003C68	E760 8EAC 0806	000010AC		3256+ VL V22, V1FUDGE	
00003C6E	E760 0200 2846			3257+ VGM V22, 2, 0, 2	test instruction (dest is a source)
00003C74	E760 5030 080E	00003C50		3258+ VST V22, V10100	save v1 output
00003C7A	07FB			3259+ BR R11	return
00003C7C				3260+RE100 DC OF	xl16 expected result
00003C7C				3261+ DROP R5	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00003C7C	BFFFFFFFF BFFFFFFFF			3262	DC	XL16' BFFFFFFFFBFFFFFFFF BFFFFFFFFBFFFFFFFF'	result
00003C84	BFFFFFFFF BFFFFFFFF						
				3263			
				3264	VRI_B	VGM 4, 0, 2	
00003C90				3265+	DS	OFD	
00003C90		00003C90		3266+	USING	*, R5	base for test data and test routine
00003C90	00003CD8			3267+T101	DC	A(X101)	address of test routine
00003C94	0065			3268+	DC	H' 101'	test number
00003C96	00			3269+	DC	X' 00'	
00003C97	02			3270+	DC	HL1' 2'	M4 field
00003C98	04			3271+	DC	HL1' 4'	i2 used
00003C99	00			3272+	DC	HL1' 0'	i3 used
00003C9A	E5C7D440 40404040			3273+	DC	CL8' VGM	instruction name
00003CA4	00003CFC			3274+	DC	A(RE101+16)	address of v2 source
00003CA8	00003D0C			3275+	DC	A(RE101+32)	address of v3 source
00003CAC	00000010			3276+	DC	A(16)	result length
00003CB0	00003CEC			3277+REA101	DC	A(RE101)	result address
00003CB8	00000000 00000000			3278+	DS	FD	gap
00003CC0	00000000 00000000			3279+V10101	DS	XL16	V1 output
00003CC8	00000000 00000000						
00003CD0	00000000 00000000			3280+	DS	FD	gap
				3281+*			
00003CD8				3282+X101	DS	OF	
00003CD8	E760 8EAC 0806		000010AC	3283+	VL	V22, V1FUDGE	
00003CDE	E760 0400 2846			3284+	VGM	V22, 4, 0, 2	test instruction (dest is a source)
00003CE4	E760 5030 080E		00003CC0	3285+	VST	V22, V10101	save v1 output
00003CEA	07FB			3286+	BR	R11	return
00003CEC				3287+RE101	DC	OF	xl16 expected result
00003CEC				3288+	DROP	R5	
00003CEC	8FFFFFFFF 8FFFFFFFF			3289	DC	XL16' 8FFFFFFFF8FFFFFFFF 8FFFFFFFF8FFFFFFFF'	result
00003CF4	8FFFFFFFF 8FFFFFFFF						
				3290			
				3291	VRI_B	VGM 6, 0, 2	
00003D00				3292+	DS	OFD	
00003D00		00003D00		3293+	USING	*, R5	base for test data and test routine
00003D00	00003D48			3294+T102	DC	A(X102)	address of test routine
00003D04	0066			3295+	DC	H' 102'	test number
00003D06	00			3296+	DC	X' 00'	
00003D07	02			3297+	DC	HL1' 2'	M4 field
00003D08	06			3298+	DC	HL1' 6'	i2 used
00003D09	00			3299+	DC	HL1' 0'	i3 used
00003D0A	E5C7D440 40404040			3300+	DC	CL8' VGM	instruction name
00003D14	00003D6C			3301+	DC	A(RE102+16)	address of v2 source
00003D18	00003D7C			3302+	DC	A(RE102+32)	address of v3 source
00003D1C	00000010			3303+	DC	A(16)	result length
00003D20	00003D5C			3304+REA102	DC	A(RE102)	result address
00003D28	00000000 00000000			3305+	DS	FD	gap
00003D30	00000000 00000000			3306+V10102	DS	XL16	V1 output
00003D38	00000000 00000000						
00003D40	00000000 00000000			3307+	DS	FD	gap
				3308+*			
00003D48				3309+X102	DS	OF	
00003D48	E760 8EAC 0806		000010AC	3310+	VL	V22, V1FUDGE	
00003D4E	E760 0600 2846			3311+	VGM	V22, 6, 0, 2	test instruction (dest is a source)
00003D54	E760 5030 080E		00003D30	3312+	VST	V22, V10102	save v1 output
00003D5A	07FB			3313+	BR	R11	return

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00003D5C				3314+RE102	DC	0F	xl16 expected result
00003D5C				3315+	DROP	R5	
00003D5C	83FFFFFF 83FFFFFF			3316	DC	XL16' 83FFFFFF83FFFFFF 83FFFFFF83FFFFFF'	result t
00003D64	83FFFFFF 83FFFFFF						
				3317			
00003D70				3318	VRI_B	VGM 7, 0, 2	
00003D70		00003D70		3319+	DS	0FD	
00003D70	00003DB8			3320+	USING	*, R5	base for test data and test routine
00003D74	0067			3321+T103	DC	A(X103)	address of test routine
00003D76	00			3322+	DC	H' 103'	test number
00003D77	02			3323+	DC	X' 00'	
00003D78	07			3324+	DC	HL1' 2'	M4 field
00003D79	00			3325+	DC	HL1' 7'	i2 used
00003D7A	E5C7D440 40404040			3326+	DC	HL1' 0'	i3 used
00003D84	00003DDC			3327+	DC	CL8' VGM	instruction name
00003D88	00003DEC			3328+	DC	A(RE103+16)	address of v2 source
00003D8C	00000010			3329+	DC	A(RE103+32)	address of v3 source
00003D90	00003DCC			3330+	DC	A(16)	result length
00003D98	00000000 00000000			3331+REA103	DC	A(RE103)	result address
00003DA0	00000000 00000000			3332+	DS	FD	gap
00003DA8	00000000 00000000			3333+V10103	DS	XL16	V1 output
00003DB0	00000000 00000000			3334+	DS	FD	gap
				3335+*			
00003DB8				3336+X103	DS	0F	
00003DB8	E760 8EAC 0806		000010AC	3337+	VL	V22, V1FUDGE	
00003DBE	E760 0700 2846			3338+	VGM	V22, 7, 0, 2	test instruction (dest is a source)
00003DC4	E760 5030 080E		00003DA0	3339+	VST	V22, V10103	save v1 output
00003DCA	07FB			3340+	BR	R11	return
00003DCC				3341+RE103	DC	0F	xl16 expected result
00003DCC				3342+	DROP	R5	
00003DCC	81FFFFFF 81FFFFFF			3343	DC	XL16' 81FFFFFF81FFFFFF 81FFFFFF81FFFFFF'	result t
00003DD4	81FFFFFF 81FFFFFF						
				3344			
00003DE0				3345	VRI_B	VGM 8, 0, 2	
00003DE0		00003DE0		3346+	DS	0FD	
00003DE0	00003E28			3347+	USING	*, R5	base for test data and test routine
00003DE4	0068			3348+T104	DC	A(X104)	address of test routine
00003DE6	00			3349+	DC	H' 104'	test number
00003DE7	02			3350+	DC	X' 00'	
00003DE8	08			3351+	DC	HL1' 2'	M4 field
00003DE9	00			3352+	DC	HL1' 8'	i2 used
00003DEA	E5C7D440 40404040			3353+	DC	HL1' 0'	i3 used
00003DEA	E5C7D440 40404040			3354+	DC	CL8' VGM	instruction name
00003DF4	00003E4C			3355+	DC	A(RE104+16)	address of v2 source
00003DF8	00003E5C			3356+	DC	A(RE104+32)	address of v3 source
00003DFC	00000010			3357+	DC	A(16)	result length
00003E00	00003E3C			3358+REA104	DC	A(RE104)	result address
00003E08	00000000 00000000			3359+	DS	FD	gap
00003E10	00000000 00000000			3360+V10104	DS	XL16	V1 output
00003E18	00000000 00000000						
00003E20	00000000 00000000			3361+	DS	FD	gap
				3362+*			
00003E28				3363+X104	DS	0F	
00003E28	E760 8EAC 0806		000010AC	3364+	VL	V22, V1FUDGE	
00003E2E	E760 0800 2846			3365+	VGM	V22, 8, 0, 2	test instruction (dest is a source)

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00003E34	E760 5030 080E		00003E10	3366+	VST	V22, V10104	save v1 output
00003E3A	07FB			3367+	BR	R11	return
00003E3C				3368+RE104	DC	0F	xl16 expected result
00003E3C				3369+	DROP	R5	
00003E3C	80FFFFFF 80FFFFFF			3370	DC	XL16' 80FFFFFF80FFFFFF 80FFFFFF80FFFFFF'	result t
00003E44	80FFFFFF 80FFFFFF						
				3371			
				3372	VRI_B	VGM 9, 0, 2	
00003E50				3373+	DS	0FD	
00003E50		00003E50		3374+	USING	*, R5	base for test data and test routine
00003E50	00003E98			3375+T105	DC	A(X105)	address of test routine
00003E54	0069			3376+	DC	H' 105'	test number
00003E56	00			3377+	DC	X' 00'	
00003E57	02			3378+	DC	HL1' 2'	M4 field
00003E58	09			3379+	DC	HL1' 9'	i2 used
00003E59	00			3380+	DC	HL1' 0'	i3 used
00003E5A	E5C7D440 40404040			3381+	DC	CL8' VGM	instruction name
00003E64	00003EBC			3382+	DC	A(RE105+16)	address of v2 source
00003E68	00003ECC			3383+	DC	A(RE105+32)	address of v3 source
00003E6C	00000010			3384+	DC	A(16)	result length
00003E70	00003EAC			3385+REA105	DC	A(RE105)	result address
00003E78	00000000 00000000			3386+	DS	FD	gap
00003E80	00000000 00000000			3387+V10105	DS	XL16	V1 output
00003E88	00000000 00000000						
00003E90	00000000 00000000			3388+	DS	FD	gap
				3389+*			
00003E98				3390+X105	DS	0F	
00003E98	E760 8EAC 0806		000010AC	3391+	VL	V22, V1FUDGE	
00003E9E	E760 0900 2846			3392+	VGM	V22, 9, 0, 2	test instruction (dest is a source)
00003EA4	E760 5030 080E		00003E80	3393+	VST	V22, V10105	save v1 output
00003EAA	07FB			3394+	BR	R11	return
00003EAC				3395+RE105	DC	0F	xl16 expected result
00003EAC				3396+	DROP	R5	
00003EAC	807FFFFFFF 807FFFFFFF			3397	DC	XL16' 807FFFFFFF807FFFFFFF 807FFFFFFF807FFFFFFF'	result t
00003EB4	807FFFFFFF 807FFFFFFF						
				3398			
				3399	VRI_B	VGM 11, 0, 2	
00003EC0				3400+	DS	0FD	
00003EC0		00003EC0		3401+	USING	*, R5	base for test data and test routine
00003EC0	00003F08			3402+T106	DC	A(X106)	address of test routine
00003EC4	006A			3403+	DC	H' 106'	test number
00003EC6	00			3404+	DC	X' 00'	
00003EC7	02			3405+	DC	HL1' 2'	M4 field
00003EC8	0B			3406+	DC	HL1' 11'	i2 used
00003EC9	00			3407+	DC	HL1' 0'	i3 used
00003ECA	E5C7D440 40404040			3408+	DC	CL8' VGM	instruction name
00003ED4	00003F2C			3409+	DC	A(RE106+16)	address of v2 source
00003ED8	00003F3C			3410+	DC	A(RE106+32)	address of v3 source
00003EDC	00000010			3411+	DC	A(16)	result length
00003EE0	00003F1C			3412+REA106	DC	A(RE106)	result address
00003EE8	00000000 00000000			3413+	DS	FD	gap
00003EF0	00000000 00000000			3414+V10106	DS	XL16	V1 output
00003EF8	00000000 00000000						
00003F00	00000000 00000000			3415+	DS	FD	gap
				3416+*			
00003F08				3417+X106	DS	0F	



LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00003F08	E760 8EAC 0806		000010AC	3418+	VL	V22, V1FUDGE	
00003F0E	E760 0B00 2846			3419+	VGM	V22, 11, 0, 2	test instruction (dest is a source)
00003F14	E760 5030 080E		00003EF0	3420+	VST	V22, V10106	save v1 output
00003F1A	07FB			3421+	BR	R11	return
00003F1C				3422+RE106	DC	0F	xl16 expected result
00003F1C				3423+	DROP	R5	
00003F1C	801FFFFFF 801FFFFFF			3424	DC	XL16' 801FFFFFF801FFFFFF 801FFFFFF801FFFFFF'	result
00003F24	801FFFFFF 801FFFFFF						
				3425			
				3426	VRI_B	VGM, 13, 0, 2	
00003F30				3427+	DS	0FD	
00003F30		00003F30		3428+	USING	*, R5	base for test data and test routine
00003F30	00003F78			3429+T107	DC	A(X107)	address of test routine
00003F34	006B			3430+	DC	H' 107'	test number
00003F36	00			3431+	DC	X' 00'	
00003F37	02			3432+	DC	HL1' 2'	M4 field
00003F38	0D			3433+	DC	HL1' 13'	i2 used
00003F39	00			3434+	DC	HL1' 0'	i3 used
00003F3A	E5C7D440 40404040			3435+	DC	CL8' VGM	instruction name
00003F44	00003F9C			3436+	DC	A(RE107+16)	address of v2 source
00003F48	00003FAC			3437+	DC	A(RE107+32)	address of v3 source
00003F4C	00000010			3438+	DC	A(16)	result length
00003F50	00003F8C			3439+REA107	DC	A(RE107)	result address
00003F58	00000000 00000000			3440+	DS	FD	gap
00003F60	00000000 00000000			3441+V10107	DS	XL16	V1 output
00003F68	00000000 00000000						
00003F70	00000000 00000000			3442+	DS	FD	gap
				3443+*			
00003F78				3444+X107	DS	0F	
00003F78	E760 8EAC 0806		000010AC	3445+	VL	V22, V1FUDGE	
00003F7E	E760 0D00 2846			3446+	VGM	V22, 13, 0, 2	test instruction (dest is a source)
00003F84	E760 5030 080E		00003F60	3447+	VST	V22, V10107	save v1 output
00003F8A	07FB			3448+	BR	R11	return
00003F8C				3449+RE107	DC	0F	xl16 expected result
00003F8C				3450+	DROP	R5	
00003F8C	8007FFFF 8007FFFF			3451	DC	XL16' 8007FFFF8007FFFF 8007FFFF8007FFFF'	result
00003F94	8007FFFF 8007FFFF						
				3452			
				3453	VRI_B	VGM, 15, 0, 2	
00003FA0				3454+	DS	0FD	
00003FA0		00003FA0		3455+	USING	*, R5	base for test data and test routine
00003FA0	00003FE8			3456+T108	DC	A(X108)	address of test routine
00003FA4	006C			3457+	DC	H' 108'	test number
00003FA6	00			3458+	DC	X' 00'	
00003FA7	02			3459+	DC	HL1' 2'	M4 field
00003FA8	0F			3460+	DC	HL1' 15'	i2 used
00003FA9	00			3461+	DC	HL1' 0'	i3 used
00003FAA	E5C7D440 40404040			3462+	DC	CL8' VGM	instruction name
00003FB4	0000400C			3463+	DC	A(RE108+16)	address of v2 source
00003FB8	0000401C			3464+	DC	A(RE108+32)	address of v3 source
00003FBC	00000010			3465+	DC	A(16)	result length
00003FC0	00003FFC			3466+REA108	DC	A(RE108)	result address
00003FC8	00000000 00000000			3467+	DS	FD	gap
00003FD0	00000000 00000000			3468+V10108	DS	XL16	V1 output
00003FD8	00000000 00000000						
00003FE0	00000000 00000000			3469+	DS	FD	gap



LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00003FE8				3470+*			
00003FE8	E760 8EAC 0806		000010AC	3471+X108	DS	0F	
00003FEE	E760 0F00 2846			3472+	VL	V22, V1FUDGE	
00003FF4	E760 5030 080E		00003FD0	3473+	VGM	V22, 15, 0, 2	test instruction (dest is a source)
00003FFA	07FB			3474+	VST	V22, V10108	save v1 output
00003FFC				3475+	BR	R11	return
00003FFC				3476+RE108	DC	0F	xl16 expected result
00003FFC	8001FFFF 8001FFFF			3477+	DROP	R5	
00004004	8001FFFF 8001FFFF			3478	DC	XL16' 8001FFFF8001FFFF 8001FFFF8001FFFF'	result t
				3479			
00004010				3480	VRI_B	VGM, 16, 0, 2	
00004010		00004010		3481+	DS	0FD	
00004010	00004058			3482+	USING	*, R5	base for test data and test routine
00004014	006D			3483+T109	DC	A(X109)	address of test routine
00004016	00			3484+	DC	H' 109'	test number
00004017	02			3485+	DC	X' 00'	
00004018	10			3486+	DC	HL1' 2'	M4 field
00004019	00			3487+	DC	HL1' 16'	i2 used
0000401A	E5C7D440 40404040			3488+	DC	HL1' 0'	i3 used
00004024	0000407C			3489+	DC	CL8' VGM	instruction name
00004028	0000408C			3490+	DC	A(RE109+16)	address of v2 source
0000402C	00000010			3491+	DC	A(RE109+32)	address of v3 source
00004030	0000406C			3492+	DC	A(16)	result length
00004038	00000000 00000000			3493+REA109	DC	A(RE109)	result address
00004040	00000000 00000000			3494+	DS	FD	gap
00004048	00000000 00000000			3495+V10109	DS	XL16	V1 output
00004050	00000000 00000000			3496+	DS	FD	gap
				3497+*			
00004058				3498+X109	DS	0F	
00004058	E760 8EAC 0806		000010AC	3499+	VL	V22, V1FUDGE	
0000405E	E760 1000 2846			3500+	VGM	V22, 16, 0, 2	test instruction (dest is a source)
00004064	E760 5030 080E		00004040	3501+	VST	V22, V10109	save v1 output
0000406A	07FB			3502+	BR	R11	return
0000406C				3503+RE109	DC	0F	xl16 expected result
0000406C				3504+	DROP	R5	
0000406C	8000FFFF 8000FFFF			3505	DC	XL16' 8000FFFF8000FFFF 8000FFFF8000FFFF'	result t
00004074	8000FFFF 8000FFFF						
				3506			
00004080				3507	VRI_B	VGM, 17, 0, 2	
00004080		00004080		3508+	DS	0FD	
00004080	000040C8			3509+	USING	*, R5	base for test data and test routine
00004084	006E			3510+T110	DC	A(X110)	address of test routine
00004086	00			3511+	DC	H' 110'	test number
00004087	02			3512+	DC	X' 00'	
00004088	11			3513+	DC	HL1' 2'	M4 field
00004089	00			3514+	DC	HL1' 17'	i2 used
0000408A	E5C7D440 40404040			3515+	DC	HL1' 0'	i3 used
00004094	000040EC			3516+	DC	CL8' VGM	instruction name
00004098	000040FC			3517+	DC	A(RE110+16)	address of v2 source
0000409C	00000010			3518+	DC	A(RE110+32)	address of v3 source
000040A0	000040DC			3519+	DC	A(16)	result length
000040A8	00000000 00000000			3520+REA110	DC	A(RE110)	result address
000040B0	00000000 00000000			3521+	DS	FD	gap
				3522+V10110	DS	XL16	V1 output

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
000040B8	00000000 00000000						
000040C0	00000000 00000000			3523+	DS	FD	gap
				3524+*			
000040C8				3525+X110	DS	0F	
000040C8	E760 8EAC 0806		000010AC	3526+	VL	V22, V1FUDGE	
000040CE	E760 1100 2846			3527+	VGM	V22, 17, 0, 2	test instruction (dest is a source)
000040D4	E760 5030 080E		000040B0	3528+	VST	V22, V10110	save v1 output
000040DA	07FB			3529+	BR	R11	return
000040DC				3530+RE110	DC	0F	xl16 expected result
000040DC				3531+	DROP	R5	
000040DC	80007FFF 80007FFF			3532	DC	XL16' 80007FFF80007FFF 80007FFF80007FFF'	result t
000040E4	80007FFF 80007FFF						
				3533			
				3534	VRI_B	VGM, 25, 0, 2	
000040F0				3535+	DS	0FD	
000040F0		000040F0		3536+	USING	*, R5	base for test data and test routine
000040F0	00004138			3537+T111	DC	A(X111)	address of test routine
000040F4	006F			3538+	DC	H' 111'	test number
000040F6	00			3539+	DC	X' 00'	
000040F7	02			3540+	DC	HL1' 2'	M4 field
000040F8	19			3541+	DC	HL1' 25'	i2 used
000040F9	00			3542+	DC	HL1' 0'	i3 used
000040FA	E5C7D440 40404040			3543+	DC	CL8' VGM	instruction name
00004104	0000415C			3544+	DC	A(RE111+16)	address of v2 source
00004108	0000416C			3545+	DC	A(RE111+32)	address of v3 source
0000410C	00000010			3546+	DC	A(16)	result length
00004110	0000414C			3547+REA111	DC	A(RE111)	result address
00004118	00000000 00000000			3548+	DS	FD	gap
00004120	00000000 00000000			3549+V10111	DS	XL16	V1 output
00004128	00000000 00000000						
00004130	00000000 00000000			3550+	DS	FD	gap
				3551+*			
00004138				3552+X111	DS	0F	
00004138	E760 8EAC 0806		000010AC	3553+	VL	V22, V1FUDGE	
0000413E	E760 1900 2846			3554+	VGM	V22, 25, 0, 2	test instruction (dest is a source)
00004144	E760 5030 080E		00004120	3555+	VST	V22, V10111	save v1 output
0000414A	07FB			3556+	BR	R11	return
0000414C				3557+RE111	DC	0F	xl16 expected result
0000414C				3558+	DROP	R5	
0000414C	8000007F 8000007F			3559	DC	XL16' 8000007F8000007F 8000007F8000007F'	result t
00004154	8000007F 8000007F						
				3560			
				3561	VRI_B	VGM, 30, 0, 2	
00004160				3562+	DS	0FD	
00004160		00004160		3563+	USING	*, R5	base for test data and test routine
00004160	000041A8			3564+T112	DC	A(X112)	address of test routine
00004164	0070			3565+	DC	H' 112'	test number
00004166	00			3566+	DC	X' 00'	
00004167	02			3567+	DC	HL1' 2'	M4 field
00004168	1E			3568+	DC	HL1' 30'	i2 used
00004169	00			3569+	DC	HL1' 0'	i3 used
0000416A	E5C7D440 40404040			3570+	DC	CL8' VGM	instruction name
00004174	000041CC			3571+	DC	A(RE112+16)	address of v2 source
00004178	000041DC			3572+	DC	A(RE112+32)	address of v3 source
0000417C	00000010			3573+	DC	A(16)	result length
00004180	000041BC			3574+REA112	DC	A(RE112)	result address

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00004188	00000000 00000000			3575+	DS	FD	gap
00004190	00000000 00000000			3576+V10112	DS	XL16	V1 output
00004198	00000000 00000000						
000041A0	00000000 00000000			3577+	DS	FD	gap
				3578+*			
000041A8				3579+X112	DS	OF	
000041A8	E760 8EAC 0806		000010AC	3580+	VL	V22, V1FUDGE	
000041AE	E760 1E00 2846			3581+	VGM	V22, 30, 0, 2	test instruction (dest is a source)
000041B4	E760 5030 080E		00004190	3582+	VST	V22, V10112	save v1 output
000041BA	07FB			3583+	BR	R11	return
000041BC				3584+RE112	DC	OF	xl16 expected result
000041BC				3585+	DROP	R5	
000041BC	80000003 80000003			3586	DC	XL16' 8000000380000003 8000000380000003'	result
000041C4	80000003 80000003						
				3587			
				3588	VRI_B	VGM 31, 0, 2	
000041D0				3589+	DS	OFD	
000041D0		000041D0		3590+	USING	*, R5	base for test data and test routine
000041D0	00004218			3591+T113	DC	A(X113)	address of test routine
000041D4	0071			3592+	DC	H' 113'	test number
000041D6	00			3593+	DC	X' 00'	
000041D7	02			3594+	DC	HL1' 2'	M4 field
000041D8	1F			3595+	DC	HL1' 31'	i2 used
000041D9	00			3596+	DC	HL1' 0'	i3 used
000041DA	E5C7D440 40404040			3597+	DC	CL8' VGM	instruction name
000041E4	0000423C			3598+	DC	A(RE113+16)	address of v2 source
000041E8	0000424C			3599+	DC	A(RE113+32)	address of v3 source
000041EC	00000010			3600+	DC	A(16)	result length
000041F0	0000422C			3601+REA113	DC	A(RE113)	result address
000041F8	00000000 00000000			3602+	DS	FD	gap
00004200	00000000 00000000			3603+V10113	DS	XL16	V1 output
00004208	00000000 00000000						
00004210	00000000 00000000			3604+	DS	FD	gap
				3605+*			
00004218				3606+X113	DS	OF	
00004218	E760 8EAC 0806		000010AC	3607+	VL	V22, V1FUDGE	
0000421E	E760 1F00 2846			3608+	VGM	V22, 31, 0, 2	test instruction (dest is a source)
00004224	E760 5030 080E		00004200	3609+	VST	V22, V10113	save v1 output
0000422A	07FB			3610+	BR	R11	return
0000422C				3611+RE113	DC	OF	xl16 expected result
0000422C				3612+	DROP	R5	
0000422C	80000001 80000001			3613	DC	XL16' 8000000180000001 8000000180000001'	result
00004234	80000001 80000001						
				3614			

LOC	OBJECT CODE	ADDR1	ADDR2	STMT	
				3616 *Word: I2>I3; I2=1	
				3617 VRI_B VGM 2, 1, 2	
00004240				3618+ DS OFD	
00004240		00004240		3619+ USING *, R5	base for test data and test routine
00004240	00004288			3620+T114 DC A(X114)	address of test routine
00004244	0072			3621+ DC H' 114'	test number
00004246	00			3622+ DC X' 00'	
00004247	02			3623+ DC HL1' 2'	M4 field
00004248	02			3624+ DC HL1' 2'	i2 used
00004249	01			3625+ DC HL1' 1'	i3 used
0000424A	E5C7D440 40404040			3626+ DC CL8' VGM	instruction name
00004254	000042AC			3627+ DC A(RE114+16)	address of v2 source
00004258	000042BC			3628+ DC A(RE114+32)	address of v3 source
0000425C	00000010			3629+ DC A(16)	result length
00004260	0000429C			3630+REA114 DC A(RE114)	result address
00004268	00000000 00000000			3631+ DS FD	gap
00004270	00000000 00000000			3632+V10114 DS XL16	V1 output
00004278	00000000 00000000				
00004280	00000000 00000000			3633+ DS FD	gap
				3634+*	
00004288				3635+X114 DS OF	
00004288	E760 8EAC 0806		000010AC	3636+ VL V22, V1FUDGE	
0000428E	E760 0201 2846			3637+ VGM V22, 2, 1, 2	test instruction (dest is a source)
00004294	E760 5030 080E		00004270	3638+ VST V22, V10114	save v1 output
0000429A	07FB			3639+ BR R11	return
0000429C				3640+RE114 DC OF	xl16 expected result
0000429C				3641+ DROP R5	
0000429C	FFFFFFFF FFFFFFFF			3642 DC XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF'	result t
000042A4	FFFFFFFF FFFFFFFF				
				3643	
				3644 VRI_B VGM 4, 1, 2	
000042B0				3645+ DS OFD	
000042B0		000042B0		3646+ USING *, R5	base for test data and test routine
000042B0	000042F8			3647+T115 DC A(X115)	address of test routine
000042B4	0073			3648+ DC H' 115'	test number
000042B6	00			3649+ DC X' 00'	
000042B7	02			3650+ DC HL1' 2'	M4 field
000042B8	04			3651+ DC HL1' 4'	i2 used
000042B9	01			3652+ DC HL1' 1'	i3 used
000042BA	E5C7D440 40404040			3653+ DC CL8' VGM	instruction name
000042C4	0000431C			3654+ DC A(RE115+16)	address of v2 source
000042C8	0000432C			3655+ DC A(RE115+32)	address of v3 source
000042CC	00000010			3656+ DC A(16)	result length
000042D0	0000430C			3657+REA115 DC A(RE115)	result address
000042D8	00000000 00000000			3658+ DS FD	gap
000042E0	00000000 00000000			3659+V10115 DS XL16	V1 output
000042E8	00000000 00000000				
000042F0	00000000 00000000			3660+ DS FD	gap
				3661+*	
000042F8				3662+X115 DS OF	
000042F8	E760 8EAC 0806		000010AC	3663+ VL V22, V1FUDGE	
000042FE	E760 0401 2846			3664+ VGM V22, 4, 1, 2	test instruction (dest is a source)
00004304	E760 5030 080E		000042E0	3665+ VST V22, V10115	save v1 output
0000430A	07FB			3666+ BR R11	return
0000430C				3667+RE115 DC OF	xl16 expected result
0000430C				3668+ DROP R5	



LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
0000430C	CFFFFFFFF CFFFFFFFF			3669	DC	XL16' CFFFFFFFFCFFFFFFFF CFFFFFFFFCFFFFFFFF'	result t
00004314	CFFFFFFFF CFFFFFFFF						
				3670			
				3671	VRI_B	VGM 6, 1, 2	
00004320				3672+	DS	OFD	
00004320		00004320		3673+	USING	*, R5	base for test data and test routine
00004320	00004368			3674+T116	DC	A(X116)	address of test routine
00004324	0074			3675+	DC	H' 116'	test number
00004326	00			3676+	DC	X' 00'	
00004327	02			3677+	DC	HL1' 2'	M4 field
00004328	06			3678+	DC	HL1' 6'	i2 used
00004329	01			3679+	DC	HL1' 1'	i3 used
0000432A	E5C7D440 40404040			3680+	DC	CL8' VGM	instruction name
00004334	0000438C			3681+	DC	A(RE116+16)	address of v2 source
00004338	0000439C			3682+	DC	A(RE116+32)	address of v3 source
0000433C	00000010			3683+	DC	A(16)	result length
00004340	0000437C			3684+REA116	DC	A(RE116)	result address
00004348	00000000 00000000			3685+	DS	FD	gap
00004350	00000000 00000000			3686+V10116	DS	XL16	V1 output
00004358	00000000 00000000						
00004360	00000000 00000000			3687+	DS	FD	gap
				3688+*			
00004368				3689+X116	DS	OF	
00004368	E760 8EAC 0806		000010AC	3690+	VL	V22, V1FUDGE	
0000436E	E760 0601 2846			3691+	VGM	V22, 6, 1, 2	test instruction (dest is a source)
00004374	E760 5030 080E		00004350	3692+	VST	V22, V10116	save v1 output
0000437A	07FB			3693+	BR	R11	return
0000437C				3694+RE116	DC	OF	xl16 expected result
0000437C				3695+	DROP	R5	
0000437C	C3FFFFFF C3FFFFFF			3696	DC	XL16' C3FFFFFFC3FFFFFF C3FFFFFFC3FFFFFF'	result t
00004384	C3FFFFFF C3FFFFFF						
				3697			
				3698	VRI_B	VGM 7, 1, 2	
00004390				3699+	DS	OFD	
00004390		00004390		3700+	USING	*, R5	base for test data and test routine
00004390	000043D8			3701+T117	DC	A(X117)	address of test routine
00004394	0075			3702+	DC	H' 117'	test number
00004396	00			3703+	DC	X' 00'	
00004397	02			3704+	DC	HL1' 2'	M4 field
00004398	07			3705+	DC	HL1' 7'	i2 used
00004399	01			3706+	DC	HL1' 1'	i3 used
0000439A	E5C7D440 40404040			3707+	DC	CL8' VGM	instruction name
000043A4	000043FC			3708+	DC	A(RE117+16)	address of v2 source
000043A8	0000440C			3709+	DC	A(RE117+32)	address of v3 source
000043AC	00000010			3710+	DC	A(16)	result length
000043B0	000043EC			3711+REA117	DC	A(RE117)	result address
000043B8	00000000 00000000			3712+	DS	FD	gap
000043C0	00000000 00000000			3713+V10117	DS	XL16	V1 output
000043C8	00000000 00000000						
000043D0	00000000 00000000			3714+	DS	FD	gap
				3715+*			
000043D8				3716+X117	DS	OF	
000043D8	E760 8EAC 0806		000010AC	3717+	VL	V22, V1FUDGE	
000043DE	E760 0701 2846			3718+	VGM	V22, 7, 1, 2	test instruction (dest is a source)
000043E4	E760 5030 080E		000043C0	3719+	VST	V22, V10117	save v1 output
000043EA	07FB			3720+	BR	R11	return



LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
000043EC				3721+RE117	DC	0F	xl16 expected result
000043EC				3722+	DROP	R5	
000043EC	C1FFFFFF C1FFFFFF			3723	DC	XL16' C1FFFFFFC1FFFFFF C1FFFFFFC1FFFFFF'	result t
000043F4	C1FFFFFF C1FFFFFF						
				3724			
				3725	VRI_B	VGM 8, 1, 2	
00004400				3726+	DS	0FD	
00004400		00004400		3727+	USING	*, R5	base for test data and test routine
00004400	00004448			3728+T118	DC	A(X118)	address of test routine
00004404	0076			3729+	DC	H' 118'	test number
00004406	00			3730+	DC	X' 00'	
00004407	02			3731+	DC	HL1' 2'	M4 field
00004408	08			3732+	DC	HL1' 8'	i2 used
00004409	01			3733+	DC	HL1' 1'	i3 used
0000440A	E5C7D440 40404040			3734+	DC	CL8' VGM	instruction name
00004414	0000446C			3735+	DC	A(RE118+16)	address of v2 source
00004418	0000447C			3736+	DC	A(RE118+32)	address of v3 source
0000441C	00000010			3737+	DC	A(16)	result length
00004420	0000445C			3738+REA118	DC	A(RE118)	result address
00004428	00000000 00000000			3739+	DS	FD	gap
00004430	00000000 00000000			3740+V10118	DS	XL16	V1 output
00004438	00000000 00000000						
00004440	00000000 00000000			3741+	DS	FD	gap
				3742+*			
00004448				3743+X118	DS	0F	
00004448	E760 8EAC 0806		000010AC	3744+	VL	V22, V1FUDGE	
0000444E	E760 0801 2846			3745+	VGM	V22, 8, 1, 2	test instruction (dest is a source)
00004454	E760 5030 080E		00004430	3746+	VST	V22, V10118	save v1 output
0000445A	07FB			3747+	BR	R11	return
0000445C				3748+RE118	DC	0F	xl16 expected result
0000445C				3749+	DROP	R5	
0000445C	C0FFFFFF C0FFFFFF			3750	DC	XL16' C0FFFFFFC0FFFFFF C0FFFFFFC0FFFFFF'	result t
00004464	C0FFFFFF C0FFFFFF						
				3751			
				3752	VRI_B	VGM 9, 1, 2	
00004470				3753+	DS	0FD	
00004470		00004470		3754+	USING	*, R5	base for test data and test routine
00004470	000044B8			3755+T119	DC	A(X119)	address of test routine
00004474	0077			3756+	DC	H' 119'	test number
00004476	00			3757+	DC	X' 00'	
00004477	02			3758+	DC	HL1' 2'	M4 field
00004478	09			3759+	DC	HL1' 9'	i2 used
00004479	01			3760+	DC	HL1' 1'	i3 used
0000447A	E5C7D440 40404040			3761+	DC	CL8' VGM	instruction name
00004484	000044DC			3762+	DC	A(RE119+16)	address of v2 source
00004488	000044EC			3763+	DC	A(RE119+32)	address of v3 source
0000448C	00000010			3764+	DC	A(16)	result length
00004490	000044CC			3765+REA119	DC	A(RE119)	result address
00004498	00000000 00000000			3766+	DS	FD	gap
000044A0	00000000 00000000			3767+V10119	DS	XL16	V1 output
000044A8	00000000 00000000						
000044B0	00000000 00000000			3768+	DS	FD	gap
				3769+*			
000044B8				3770+X119	DS	0F	
000044B8	E760 8EAC 0806		000010AC	3771+	VL	V22, V1FUDGE	
000044BE	E760 0901 2846			3772+	VGM	V22, 9, 1, 2	test instruction (dest is a source)

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
000044C4	E760 5030 080E		000044A0	3773+	VST	V22, V10119	save v1 output
000044CA	07FB			3774+	BR	R11	return
000044CC				3775+RE119	DC	0F	xl16 expected result
000044CC				3776+	DROP	R5	
000044CC	C07FFFFFFF C07FFFFFFF			3777	DC	XL16' C07FFFFFFFC07FFFFFF C07FFFFFFC07FFFFFF'	result t
000044D4	C07FFFFFFF C07FFFFFFF						
				3778			
				3779	VRI_B	VGM, 11, 1, 2	
000044E0				3780+	DS	0FD	
000044E0		000044E0		3781+	USING	*, R5	base for test data and test routine
000044E0	00004528			3782+T120	DC	A(X120)	address of test routine
000044E4	0078			3783+	DC	H' 120'	test number
000044E6	00			3784+	DC	X' 00'	
000044E7	02			3785+	DC	HL1' 2'	M4 field
000044E8	0B			3786+	DC	HL1' 11'	i2 used
000044E9	01			3787+	DC	HL1' 1'	i3 used
000044EA	E5C7D440 40404040			3788+	DC	CL8' VGM	instruction name
000044F4	0000454C			3789+	DC	A(RE120+16)	address of v2 source
000044F8	0000455C			3790+	DC	A(RE120+32)	address of v3 source
000044FC	00000010			3791+	DC	A(16)	result length
00004500	0000453C			3792+REA120	DC	A(RE120)	result address
00004508	00000000 00000000			3793+	DS	FD	gap
00004510	00000000 00000000			3794+V10120	DS	XL16	V1 output
00004518	00000000 00000000						
00004520	00000000 00000000			3795+	DS	FD	gap
				3796+*			
00004528				3797+X120	DS	0F	
00004528	E760 8EAC 0806		000010AC	3798+	VL	V22, V1FUDGE	
0000452E	E760 0B01 2846			3799+	VGM	V22, 11, 1, 2	test instruction (dest is a source)
00004534	E760 5030 080E		00004510	3800+	VST	V22, V10120	save v1 output
0000453A	07FB			3801+	BR	R11	return
0000453C				3802+RE120	DC	0F	xl16 expected result
0000453C				3803+	DROP	R5	
0000453C	C01FFFFFFF C01FFFFFFF			3804	DC	XL16' C01FFFFFFFC01FFFFFF C01FFFFFFC01FFFFFF'	result t
00004544	C01FFFFFFF C01FFFFFFF						
				3805			
				3806	VRI_B	VGM, 13, 1, 2	
00004550				3807+	DS	0FD	
00004550		00004550		3808+	USING	*, R5	base for test data and test routine
00004550	00004598			3809+T121	DC	A(X121)	address of test routine
00004554	0079			3810+	DC	H' 121'	test number
00004556	00			3811+	DC	X' 00'	
00004557	02			3812+	DC	HL1' 2'	M4 field
00004558	0D			3813+	DC	HL1' 13'	i2 used
00004559	01			3814+	DC	HL1' 1'	i3 used
0000455A	E5C7D440 40404040			3815+	DC	CL8' VGM	instruction name
00004564	000045BC			3816+	DC	A(RE121+16)	address of v2 source
00004568	000045CC			3817+	DC	A(RE121+32)	address of v3 source
0000456C	00000010			3818+	DC	A(16)	result length
00004570	000045AC			3819+REA121	DC	A(RE121)	result address
00004578	00000000 00000000			3820+	DS	FD	gap
00004580	00000000 00000000			3821+V10121	DS	XL16	V1 output
00004588	00000000 00000000						
00004590	00000000 00000000			3822+	DS	FD	gap
				3823+*			
00004598				3824+X121	DS	0F	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00004598	E760 8EAC 0806		000010AC	3825+	VL	V22, V1FUDGE	
0000459E	E760 0D01 2846			3826+	VGM	V22, 13, 1, 2	test instruction (dest is a source)
000045A4	E760 5030 080E		00004580	3827+	VST	V22, V10121	save v1 output
000045AA	07FB			3828+	BR	R11	return
000045AC				3829+RE121	DC	0F	xl16 expected result
000045AC				3830+	DROP	R5	
000045AC	C007FFFF C007FFFF			3831	DC	XL16' C007FFFFC007FFFF C007FFFFC007FFFF'	result t
000045B4	C007FFFF C007FFFF						
				3832			
				3833	VRI_B	VGM, 15, 1, 2	
000045C0				3834+	DS	0FD	
000045C0		000045C0		3835+	USING	*, R5	base for test data and test routine
000045C0	00004608			3836+T122	DC	A(X122)	address of test routine
000045C4	007A			3837+	DC	H' 122'	test number
000045C6	00			3838+	DC	X' 00'	
000045C7	02			3839+	DC	HL1' 2'	M4 field
000045C8	0F			3840+	DC	HL1' 15'	i2 used
000045C9	01			3841+	DC	HL1' 1'	i3 used
000045CA	E5C7D440 40404040			3842+	DC	CL8' VGM	instruction name
000045D4	0000462C			3843+	DC	A(RE122+16)	address of v2 source
000045D8	0000463C			3844+	DC	A(RE122+32)	address of v3 source
000045DC	00000010			3845+	DC	A(16)	result length
000045E0	0000461C			3846+REA122	DC	A(RE122)	result address
000045E8	00000000 00000000			3847+	DS	FD	gap
000045F0	00000000 00000000			3848+V10122	DS	XL16	V1 output
000045F8	00000000 00000000						
00004600	00000000 00000000			3849+	DS	FD	gap
				3850+*			
00004608				3851+X122	DS	0F	
00004608	E760 8EAC 0806		000010AC	3852+	VL	V22, V1FUDGE	
0000460E	E760 0F01 2846			3853+	VGM	V22, 15, 1, 2	test instruction (dest is a source)
00004614	E760 5030 080E		000045F0	3854+	VST	V22, V10122	save v1 output
0000461A	07FB			3855+	BR	R11	return
0000461C				3856+RE122	DC	0F	xl16 expected result
0000461C				3857+	DROP	R5	
0000461C	C001FFFF C001FFFF			3858	DC	XL16' C001FFFFC001FFFF C001FFFFC001FFFF'	result t
00004624	C001FFFF C001FFFF						
				3859			
				3860	VRI_B	VGM, 16, 1, 2	
00004630				3861+	DS	0FD	
00004630		00004630		3862+	USING	*, R5	base for test data and test routine
00004630	00004678			3863+T123	DC	A(X123)	address of test routine
00004634	007B			3864+	DC	H' 123'	test number
00004636	00			3865+	DC	X' 00'	
00004637	02			3866+	DC	HL1' 2'	M4 field
00004638	10			3867+	DC	HL1' 16'	i2 used
00004639	01			3868+	DC	HL1' 1'	i3 used
0000463A	E5C7D440 40404040			3869+	DC	CL8' VGM	instruction name
00004644	0000469C			3870+	DC	A(RE123+16)	address of v2 source
00004648	000046AC			3871+	DC	A(RE123+32)	address of v3 source
0000464C	00000010			3872+	DC	A(16)	result length
00004650	0000468C			3873+REA123	DC	A(RE123)	result address
00004658	00000000 00000000			3874+	DS	FD	gap
00004660	00000000 00000000			3875+V10123	DS	XL16	V1 output
00004668	00000000 00000000						
00004670	00000000 00000000			3876+	DS	FD	gap

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00004678				3877+*			
00004678	E760 8EAC 0806		000010AC	3878+X123	DS	0F	
0000467E	E760 1001 2846			3879+	VL	V22, V1FUDGE	
00004684	E760 5030 080E		00004660	3880+	VGM	V22, 16, 1, 2	test instruction (dest is a source)
0000468A	07FB			3881+	VST	V22, V10123	save v1 output
0000468C				3882+	BR	R11	return
0000468C				3883+RE123	DC	0F	xl16 expected result
0000468C				3884+	DROP	R5	
0000468C	C000FFFF C000FFFF			3885	DC	XL16' C000FFFFC000FFFF C000FFFFC000FFFF'	result t
00004694	C000FFFF C000FFFF						
000046A0				3886			
000046A0		000046A0		3887	VRI_B	VGM, 17, 1, 2	
000046A0	000046E8			3888+	DS	0FD	
000046A4	007C			3889+	USING	*, R5	base for test data and test routine
000046A6	00			3890+T124	DC	A(X124)	address of test routine
000046A7	02			3891+	DC	H' 124'	test number
000046A8	11			3892+	DC	X' 00'	
000046A9	01			3893+	DC	HL1' 2'	M4 field
000046AA	E5C7D440 40404040			3894+	DC	HL1' 17'	i2 used
000046B4	0000470C			3895+	DC	HL1' 1'	i3 used
000046B8	0000471C			3896+	DC	CL8' VGM	instruction name
000046BC	00000010			3897+	DC	A(RE124+16)	address of v2 source
000046C0	000046FC			3898+	DC	A(RE124+32)	address of v3 source
000046C8	00000000 00000000			3899+	DC	A(16)	result length
000046D0	00000000 00000000			3900+REA124	DC	A(RE124)	result address
000046D8	00000000 00000000			3901+	DS	FD	gap
000046E0	00000000 00000000			3902+V10124	DS	XL16	V1 output
000046E8				3903+	DS	FD	gap
000046E8	E760 8EAC 0806		000010AC	3904+*			
000046E8	E760 1101 2846			3905+X124	DS	0F	
000046EE	E760 5030 080E		000046D0	3906+	VL	V22, V1FUDGE	
000046FA	07FB			3907+	VGM	V22, 17, 1, 2	test instruction (dest is a source)
000046FC				3908+	VST	V22, V10124	save v1 output
000046FC				3909+	BR	R11	return
000046FC				3910+RE124	DC	0F	xl16 expected result
000046FC	C0007FFF C0007FFF			3911+	DROP	R5	
00004704	C0007FFF C0007FFF			3912	DC	XL16' C0007FFFC0007FFF C0007FFFC0007FFF'	result t
00004710				3913			
00004710		00004710		3914	VRI_B	VGM, 25, 1, 2	
00004710	00004758			3915+	DS	0FD	
00004714	007D			3916+	USING	*, R5	base for test data and test routine
00004716	00			3917+T125	DC	A(X125)	address of test routine
00004717	02			3918+	DC	H' 125'	test number
00004718	19			3919+	DC	X' 00'	
00004719	01			3920+	DC	HL1' 2'	M4 field
0000471A	E5C7D440 40404040			3921+	DC	HL1' 25'	i2 used
00004724	0000477C			3922+	DC	HL1' 1'	i3 used
00004728	0000478C			3923+	DC	CL8' VGM	instruction name
0000472C	00000010			3924+	DC	A(RE125+16)	address of v2 source
00004730	0000476C			3925+	DC	A(RE125+32)	address of v3 source
00004738	00000000 00000000			3926+	DC	A(16)	result length
00004740	00000000 00000000			3927+REA125	DC	A(RE125)	result address
				3928+	DS	FD	gap
				3929+V10125	DS	XL16	V1 output



LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00004748	00000000 00000000						
00004750	00000000 00000000			3930+	DS	FD	gap
				3931+*			
00004758				3932+X125	DS	0F	
00004758	E760 8EAC 0806		000010AC	3933+	VL	V22, V1FUDGE	
0000475E	E760 1901 2846			3934+	VGM	V22, 25, 1, 2	test instruction (dest is a source)
00004764	E760 5030 080E		00004740	3935+	VST	V22, V10125	save v1 output
0000476A	07FB			3936+	BR	R11	return
0000476C				3937+RE125	DC	0F	xl16 expected result
0000476C				3938+	DROP	R5	
0000476C	C000007F C000007F			3939	DC	XL16' C000007FC000007F C000007FC000007F'	result t
00004774	C000007F C000007F						
				3940			
				3941	VRI_B	VGM, 30, 1, 2	
00004780				3942+	DS	0FD	
00004780		00004780		3943+	USING	*, R5	base for test data and test routine
00004780	000047C8			3944+T126	DC	A(X126)	address of test routine
00004784	007E			3945+	DC	H' 126'	test number
00004786	00			3946+	DC	X' 00'	
00004787	02			3947+	DC	HL1' 2'	M4 field
00004788	1E			3948+	DC	HL1' 30'	i2 used
00004789	01			3949+	DC	HL1' 1'	i3 used
0000478A	E5C7D440 40404040			3950+	DC	CL8' VGM	instruction name
00004794	000047EC			3951+	DC	A(RE126+16)	address of v2 source
00004798	000047FC			3952+	DC	A(RE126+32)	address of v3 source
0000479C	00000010			3953+	DC	A(16)	result length
000047A0	000047DC			3954+REA126	DC	A(RE126)	result address
000047A8	00000000 00000000			3955+	DS	FD	gap
000047B0	00000000 00000000			3956+V10126	DS	XL16	V1 output
000047B8	00000000 00000000						
000047C0	00000000 00000000			3957+	DS	FD	gap
				3958+*			
000047C8				3959+X126	DS	0F	
000047C8	E760 8EAC 0806		000010AC	3960+	VL	V22, V1FUDGE	
000047CE	E760 1E01 2846			3961+	VGM	V22, 30, 1, 2	test instruction (dest is a source)
000047D4	E760 5030 080E		000047B0	3962+	VST	V22, V10126	save v1 output
000047DA	07FB			3963+	BR	R11	return
000047DC				3964+RE126	DC	0F	xl16 expected result
000047DC				3965+	DROP	R5	
000047DC	C0000003 C0000003			3966	DC	XL16' C0000003C0000003 C0000003C0000003'	result t
000047E4	C0000003 C0000003						
				3967			
				3968	VRI_B	VGM, 31, 1, 2	
000047F0				3969+	DS	0FD	
000047F0		000047F0		3970+	USING	*, R5	base for test data and test routine
000047F0	00004838			3971+T127	DC	A(X127)	address of test routine
000047F4	007F			3972+	DC	H' 127'	test number
000047F6	00			3973+	DC	X' 00'	
000047F7	02			3974+	DC	HL1' 2'	M4 field
000047F8	1F			3975+	DC	HL1' 31'	i2 used
000047F9	01			3976+	DC	HL1' 1'	i3 used
000047FA	E5C7D440 40404040			3977+	DC	CL8' VGM	instruction name
00004804	0000485C			3978+	DC	A(RE127+16)	address of v2 source
00004808	0000486C			3979+	DC	A(RE127+32)	address of v3 source
0000480C	00000010			3980+	DC	A(16)	result length
00004810	0000484C			3981+REA127	DC	A(RE127)	result address





LOC	OBJECT CODE	ADDR1	ADDR2	STMT	
				3996 *Doubleword: I2<I3; I2=0	
				3997 VRI_B VGM 0, 0, 3	
00004860				3998+ DS OFD	
00004860		00004860		3999+ USING *, R5	base for test data and test routine
00004860	000048A8			4000+T128 DC A(X128)	address of test routine
00004864	0080			4001+ DC H' 128'	test number
00004866	00			4002+ DC X' 00'	
00004867	03			4003+ DC HL1' 3'	M4 field
00004868	00			4004+ DC HL1' 0'	i2 used
00004869	00			4005+ DC HL1' 0'	i3 used
0000486A	E5C7D440 40404040			4006+ DC CL8' VGM	instruction name
00004874	000048CC			4007+ DC A(RE128+16)	address of v2 source
00004878	000048DC			4008+ DC A(RE128+32)	address of v3 source
0000487C	00000010			4009+ DC A(16)	result length
00004880	000048BC			4010+REA128 DC A(RE128)	result address
00004888	00000000 00000000			4011+ DS FD	gap
00004890	00000000 00000000			4012+V10128 DS XL16	V1 output
00004898	00000000 00000000				
000048A0	00000000 00000000			4013+ DS FD	gap
				4014+*	
000048A8				4015+X128 DS OF	
000048A8	E760 8EAC 0806		000010AC	4016+ VL V22, V1FUDGE	
000048AE	E760 0000 3846			4017+ VGM V22, 0, 0, 3	test instruction (dest is a source)
000048B4	E760 5030 080E		00004890	4018+ VST V22, V10128	save v1 output
000048BA	07FB			4019+ BR R11	return
000048BC				4020+RE128 DC OF	xl16 expected result
000048BC				4021+ DROP R5	
000048BC	80000000 00000000			4022 DC XL16' 8000000000000000 8000000000000000'	result
000048C4	80000000 00000000				
				4023	
				4024 VRI_B VGM 0, 1, 3	
000048D0				4025+ DS OFD	
000048D0		000048D0		4026+ USING *, R5	base for test data and test routine
000048D0	00004918			4027+T129 DC A(X129)	address of test routine
000048D4	0081			4028+ DC H' 129'	test number
000048D6	00			4029+ DC X' 00'	
000048D7	03			4030+ DC HL1' 3'	M4 field
000048D8	00			4031+ DC HL1' 0'	i2 used
000048D9	01			4032+ DC HL1' 1'	i3 used
000048DA	E5C7D440 40404040			4033+ DC CL8' VGM	instruction name
000048E4	0000493C			4034+ DC A(RE129+16)	address of v2 source
000048E8	0000494C			4035+ DC A(RE129+32)	address of v3 source
000048EC	00000010			4036+ DC A(16)	result length
000048F0	0000492C			4037+REA129 DC A(RE129)	result address
000048F8	00000000 00000000			4038+ DS FD	gap
00004900	00000000 00000000			4039+V10129 DS XL16	V1 output
00004908	00000000 00000000				
00004910	00000000 00000000			4040+ DS FD	gap
				4041+*	
00004918				4042+X129 DS OF	
00004918	E760 8EAC 0806		000010AC	4043+ VL V22, V1FUDGE	
0000491E	E760 0001 3846			4044+ VGM V22, 0, 1, 3	test instruction (dest is a source)
00004924	E760 5030 080E		00004900	4045+ VST V22, V10129	save v1 output
0000492A	07FB			4046+ BR R11	return
0000492C				4047+RE129 DC OF	xl16 expected result
0000492C				4048+ DROP R5	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
0000492C	C0000000 00000000			4049	DC	XL16' C000000000000000 C000000000000000'	result
00004934	C0000000 00000000						
				4050			
				4051	VRI_B	VGM 0, 2, 3	
00004940				4052+	DS	OFD	
00004940		00004940		4053+	USING	*, R5	base for test data and test routine
00004940	00004988			4054+T130	DC	A(X130)	address of test routine
00004944	0082			4055+	DC	H' 130'	test number
00004946	00			4056+	DC	X' 00'	
00004947	03			4057+	DC	HL1' 3'	M4 field
00004948	00			4058+	DC	HL1' 0'	i2 used
00004949	02			4059+	DC	HL1' 2'	i3 used
0000494A	E5C7D440 40404040			4060+	DC	CL8' VGM	instruction name
00004954	000049AC			4061+	DC	A(RE130+16)	address of v2 source
00004958	000049BC			4062+	DC	A(RE130+32)	address of v3 source
0000495C	00000010			4063+	DC	A(16)	result length
00004960	0000499C			4064+REA130	DC	A(RE130)	result address
00004968	00000000 00000000			4065+	DS	FD	gap
00004970	00000000 00000000			4066+V10130	DS	XL16	V1 output
00004978	00000000 00000000						
00004980	00000000 00000000			4067+	DS	FD	gap
				4068+*			
00004988				4069+X130	DS	OF	
00004988	E760 8EAC 0806		000010AC	4070+	VL	V22, V1FUDGE	
0000498E	E760 0002 3846			4071+	VGM	V22, 0, 2, 3	test instruction (dest is a source)
00004994	E760 5030 080E		00004970	4072+	VST	V22, V10130	save v1 output
0000499A	07FB			4073+	BR	R11	return
0000499C				4074+RE130	DC	OF	xl16 expected result
0000499C				4075+	DROP	R5	
0000499C	E0000000 00000000			4076	DC	XL16' E000000000000000 E000000000000000'	result
000049A4	E0000000 00000000						
				4077			
				4078	VRI_B	VGM 0, 4, 3	
000049B0				4079+	DS	OFD	
000049B0		000049B0		4080+	USING	*, R5	base for test data and test routine
000049B0	000049F8			4081+T131	DC	A(X131)	address of test routine
000049B4	0083			4082+	DC	H' 131'	test number
000049B6	00			4083+	DC	X' 00'	
000049B7	03			4084+	DC	HL1' 3'	M4 field
000049B8	00			4085+	DC	HL1' 0'	i2 used
000049B9	04			4086+	DC	HL1' 4'	i3 used
000049BA	E5C7D440 40404040			4087+	DC	CL8' VGM	instruction name
000049C4	00004A1C			4088+	DC	A(RE131+16)	address of v2 source
000049C8	00004A2C			4089+	DC	A(RE131+32)	address of v3 source
000049CC	00000010			4090+	DC	A(16)	result length
000049D0	00004A0C			4091+REA131	DC	A(RE131)	result address
000049D8	00000000 00000000			4092+	DS	FD	gap
000049E0	00000000 00000000			4093+V10131	DS	XL16	V1 output
000049E8	00000000 00000000						
000049F0	00000000 00000000			4094+	DS	FD	gap
				4095+*			
000049F8				4096+X131	DS	OF	
000049F8	E760 8EAC 0806		000010AC	4097+	VL	V22, V1FUDGE	
000049FE	E760 0004 3846			4098+	VGM	V22, 0, 4, 3	test instruction (dest is a source)
00004A04	E760 5030 080E		000049E0	4099+	VST	V22, V10131	save v1 output
00004A0A	07FB			4100+	BR	R11	return

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00004A0C				4101+RE131	DC	0F	xl16 expected result
00004A0C				4102+	DROP	R5	
00004A0C	F8000000 00000000			4103	DC	XL16' F800000000000000 F800000000000000'	result
00004A14	F8000000 00000000						
				4104			
00004A20				4105	VRI_B	VGM 0, 7, 3	
00004A20		00004A20		4106+	DS	0FD	
00004A20	00004A68			4107+	USING	*, R5	base for test data and test routine
00004A24	0084			4108+T132	DC	A(X132)	address of test routine
00004A26	00			4109+	DC	H' 132'	test number
00004A26	00			4110+	DC	X' 00'	
00004A27	03			4111+	DC	HL1' 3'	M4 field
00004A28	00			4112+	DC	HL1' 0'	i2 used
00004A29	07			4113+	DC	HL1' 7'	i3 used
00004A2A	E5C7D440 40404040			4114+	DC	CL8' VGM	instruction name
00004A34	00004A8C			4115+	DC	A(RE132+16)	address of v2 source
00004A38	00004A9C			4116+	DC	A(RE132+32)	address of v3 source
00004A3C	00000010			4117+	DC	A(16)	result length
00004A40	00004A7C			4118+REA132	DC	A(RE132)	result address
00004A48	00000000 00000000			4119+	DS	FD	gap
00004A50	00000000 00000000			4120+V10132	DS	XL16	V1 output
00004A58	00000000 00000000						
00004A60	00000000 00000000			4121+	DS	FD	gap
				4122+*			
00004A68				4123+X132	DS	0F	
00004A68	E760 8EAC 0806		000010AC	4124+	VL	V22, V1FUDGE	
00004A6E	E760 0007 3846			4125+	VGM	V22, 0, 7, 3	test instruction (dest is a source)
00004A74	E760 5030 080E		00004A50	4126+	VST	V22, V10132	save v1 output
00004A7A	07FB			4127+	BR	R11	return
00004A7C				4128+RE132	DC	0F	xl16 expected result
00004A7C				4129+	DROP	R5	
00004A7C	FF000000 00000000			4130	DC	XL16' FF00000000000000 FF00000000000000'	result
00004A84	FF000000 00000000						
				4131			
00004A90				4132	VRI_B	VGM 0, 8, 3	
00004A90		00004A90		4133+	DS	0FD	
00004A90	00004AD8			4134+	USING	*, R5	base for test data and test routine
00004A94	0085			4135+T133	DC	A(X133)	address of test routine
00004A96	00			4136+	DC	H' 133'	test number
00004A96	00			4137+	DC	X' 00'	
00004A97	03			4138+	DC	HL1' 3'	M4 field
00004A98	00			4139+	DC	HL1' 0'	i2 used
00004A99	08			4140+	DC	HL1' 8'	i3 used
00004A9A	E5C7D440 40404040			4141+	DC	CL8' VGM	instruction name
00004AA4	00004AFC			4142+	DC	A(RE133+16)	address of v2 source
00004AA8	00004B0C			4143+	DC	A(RE133+32)	address of v3 source
00004AAC	00000010			4144+	DC	A(16)	result length
00004AB0	00004AEC			4145+REA133	DC	A(RE133)	result address
00004AB8	00000000 00000000			4146+	DS	FD	gap
00004AC0	00000000 00000000			4147+V10133	DS	XL16	V1 output
00004AC8	00000000 00000000						
00004AD0	00000000 00000000			4148+	DS	FD	gap
				4149+*			
00004AD8				4150+X133	DS	0F	
00004AD8	E760 8EAC 0806		000010AC	4151+	VL	V22, V1FUDGE	
00004ADE	E760 0008 3846			4152+	VGM	V22, 0, 8, 3	test instruction (dest is a source)

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00004AE4	E760 5030 080E		00004AC0	4153+	VST	V22, V10133	save v1 output
00004AEA	07FB			4154+	BR	R11	return
00004AEC				4155+RE133	DC	0F	xl16 expected result
00004AEC				4156+	DROP	R5	
00004AEC	FF800000 00000000			4157	DC	XL16' FF80000000000000 FF80000000000000'	result t
00004AF4	FF800000 00000000						
				4158			
				4159	VRI_B	VGM 0, 9, 3	
00004B00				4160+	DS	0FD	
00004B00		00004B00		4161+	USING	*, R5	base for test data and test routine
00004B00	00004B48			4162+T134	DC	A(X134)	address of test routine
00004B04	0086			4163+	DC	H' 134'	test number
00004B06	00			4164+	DC	X' 00'	
00004B07	03			4165+	DC	HL1' 3'	M4 field
00004B08	00			4166+	DC	HL1' 0'	i2 used
00004B09	09			4167+	DC	HL1' 9'	i3 used
00004B0A	E5C7D440 40404040			4168+	DC	CL8' VGM	instruction name
00004B14	00004B6C			4169+	DC	A(RE134+16)	address of v2 source
00004B18	00004B7C			4170+	DC	A(RE134+32)	address of v3 source
00004B1C	00000010			4171+	DC	A(16)	result length
00004B20	00004B5C			4172+REA134	DC	A(RE134)	result address
00004B28	00000000 00000000			4173+	DS	FD	gap
00004B30	00000000 00000000			4174+V10134	DS	XL16	V1 output
00004B38	00000000 00000000						
00004B40	00000000 00000000			4175+	DS	FD	gap
				4176+*			
00004B48				4177+X134	DS	0F	
00004B48	E760 8EAC 0806		000010AC	4178+	VL	V22, V1FUDGE	
00004B4E	E760 0009 3846			4179+	VGM	V22, 0, 9, 3	test instruction (dest is a source)
00004B54	E760 5030 080E		00004B30	4180+	VST	V22, V10134	save v1 output
00004B5A	07FB			4181+	BR	R11	return
00004B5C				4182+RE134	DC	0F	xl16 expected result
00004B5C				4183+	DROP	R5	
00004B5C	FFC00000 00000000			4184	DC	XL16' FFC0000000000000 FFC0000000000000'	result t
00004B64	FFC00000 00000000						
				4185			
				4186	VRI_B	VGM 0, 13, 3	
00004B70				4187+	DS	0FD	
00004B70		00004B70		4188+	USING	*, R5	base for test data and test routine
00004B70	00004BB8			4189+T135	DC	A(X135)	address of test routine
00004B74	0087			4190+	DC	H' 135'	test number
00004B76	00			4191+	DC	X' 00'	
00004B77	03			4192+	DC	HL1' 3'	M4 field
00004B78	00			4193+	DC	HL1' 0'	i2 used
00004B79	0D			4194+	DC	HL1' 13'	i3 used
00004B7A	E5C7D440 40404040			4195+	DC	CL8' VGM	instruction name
00004B84	00004BDC			4196+	DC	A(RE135+16)	address of v2 source
00004B88	00004BEC			4197+	DC	A(RE135+32)	address of v3 source
00004B8C	00000010			4198+	DC	A(16)	result length
00004B90	00004BCC			4199+REA135	DC	A(RE135)	result address
00004B98	00000000 00000000			4200+	DS	FD	gap
00004BA0	00000000 00000000			4201+V10135	DS	XL16	V1 output
00004BA8	00000000 00000000						
00004BB0	00000000 00000000			4202+	DS	FD	gap
				4203+*			
00004BB8				4204+X135	DS	0F	



LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00004BB8	E760 8EAC 0806		000010AC	4205+	VL	V22, V1FUDGE	
00004BBE	E760 000D 3846			4206+	VGM	V22, 0, 13, 3	test instruction (dest is a source)
00004BC4	E760 5030 080E		00004BA0	4207+	VST	V22, V10135	save v1 output
00004BCA	07FB			4208+	BR	R11	return
00004BCC				4209+RE135	DC	0F	xl16 expected result
00004BCC				4210+	DROP	R5	
00004BCC	FFFC0000 00000000			4211	DC	XL16' FFFC000000000000 FFFC000000000000'	result
00004BD4	FFFC0000 00000000						
				4212			
				4213	VRI_B	VGM, 0, 15, 3	
00004BE0				4214+	DS	0FD	
00004BE0		00004BE0		4215+	USING	*, R5	base for test data and test routine
00004BE0	00004C28			4216+T136	DC	A(X136)	address of test routine
00004BE4	0088			4217+	DC	H' 136'	test number
00004BE6	00			4218+	DC	X' 00'	
00004BE7	03			4219+	DC	HL1' 3'	M4 field
00004BE8	00			4220+	DC	HL1' 0'	i2 used
00004BE9	0F			4221+	DC	HL1' 15'	i3 used
00004BEA	E5C7D440 40404040			4222+	DC	CL8' VGM	instruction name
00004BF4	00004C4C			4223+	DC	A(RE136+16)	address of v2 source
00004BF8	00004C5C			4224+	DC	A(RE136+32)	address of v3 source
00004BFC	00000010			4225+	DC	A(16)	result length
00004C00	00004C3C			4226+REA136	DC	A(RE136)	result address
00004C08	00000000 00000000			4227+	DS	FD	gap
00004C10	00000000 00000000			4228+V10136	DS	XL16	V1 output
00004C18	00000000 00000000						
00004C20	00000000 00000000			4229+	DS	FD	gap
				4230+*			
00004C28				4231+X136	DS	0F	
00004C28	E760 8EAC 0806		000010AC	4232+	VL	V22, V1FUDGE	
00004C2E	E760 000F 3846			4233+	VGM	V22, 0, 15, 3	test instruction (dest is a source)
00004C34	E760 5030 080E		00004C10	4234+	VST	V22, V10136	save v1 output
00004C3A	07FB			4235+	BR	R11	return
00004C3C				4236+RE136	DC	0F	xl16 expected result
00004C3C				4237+	DROP	R5	
00004C3C	FFFF0000 00000000			4238	DC	XL16' FFFF000000000000 FFFF000000000000'	result
00004C44	FFFF0000 00000000						
				4239			
				4240	VRI_B	VGM, 0, 16, 3	
00004C50				4241+	DS	0FD	
00004C50		00004C50		4242+	USING	*, R5	base for test data and test routine
00004C50	00004C98			4243+T137	DC	A(X137)	address of test routine
00004C54	0089			4244+	DC	H' 137'	test number
00004C56	00			4245+	DC	X' 00'	
00004C57	03			4246+	DC	HL1' 3'	M4 field
00004C58	00			4247+	DC	HL1' 0'	i2 used
00004C59	10			4248+	DC	HL1' 16'	i3 used
00004C5A	E5C7D440 40404040			4249+	DC	CL8' VGM	instruction name
00004C64	00004CBC			4250+	DC	A(RE137+16)	address of v2 source
00004C68	00004CCC			4251+	DC	A(RE137+32)	address of v3 source
00004C6C	00000010			4252+	DC	A(16)	result length
00004C70	00004CAC			4253+REA137	DC	A(RE137)	result address
00004C78	00000000 00000000			4254+	DS	FD	gap
00004C80	00000000 00000000			4255+V10137	DS	XL16	V1 output
00004C88	00000000 00000000						
00004C90	00000000 00000000			4256+	DS	FD	gap

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00004C98				4257+*			
00004C98	E760 8EAC 0806		000010AC	4258+X137	DS	0F	
00004C9E	E760 0010 3846			4259+	VL	V22, V1FUDGE	
00004CA4	E760 5030 080E		00004C80	4260+	VGM	V22, 0, 16, 3	test instruction (dest is a source)
00004CAA	07FB			4261+	VST	V22, V10137	save v1 output
00004CAC				4262+	BR	R11	return
00004CAC				4263+RE137	DC	0F	xl16 expected result
00004CAC	FFFF8000 00000000			4264+	DROP	R5	
00004CB4	FFFF8000 00000000			4265	DC	XL16' FFFF800000000000 FFFF800000000000'	result
				4266			
00004CC0				4267	VRI_B	VGM 0, 17, 3	
00004CC0		00004CC0		4268+	DS	0FD	
00004CC0	00004D08			4269+	USING	*, R5	base for test data and test routine
00004CC4	008A			4270+T138	DC	A(X138)	address of test routine
00004CC6	00			4271+	DC	H' 138'	test number
00004CC7	03			4272+	DC	X' 00'	
00004CC8	00			4273+	DC	HL1' 3'	M4 field
00004CC9	11			4274+	DC	HL1' 0'	i2 used
00004CCA	E5C7D440 40404040			4275+	DC	HL1' 17'	i3 used
00004CD4	00004D2C			4276+	DC	CL8' VGM	instruction name
00004CD8	00004D3C			4277+	DC	A(RE138+16)	address of v2 source
00004CDC	00000010			4278+	DC	A(RE138+32)	address of v3 source
00004CE0	00004D1C			4279+	DC	A(16)	result length
00004CE8	00000000 00000000			4280+REA138	DC	A(RE138)	result address
00004CF0	00000000 00000000			4281+	DS	FD	gap
00004CF8	00000000 00000000			4282+V10138	DS	XL16	V1 output
00004D00	00000000 00000000			4283+	DS	FD	gap
				4284+*			
00004D08				4285+X138	DS	0F	
00004D08	E760 8EAC 0806		000010AC	4286+	VL	V22, V1FUDGE	
00004D0E	E760 0011 3846			4287+	VGM	V22, 0, 17, 3	test instruction (dest is a source)
00004D14	E760 5030 080E		00004CF0	4288+	VST	V22, V10138	save v1 output
00004D1A	07FB			4289+	BR	R11	return
00004D1C				4290+RE138	DC	0F	xl16 expected result
00004D1C				4291+	DROP	R5	
00004D1C	FFFFC000 00000000			4292	DC	XL16' FFFFC00000000000 FFFFC00000000000'	result
00004D24	FFFFC000 00000000						
				4293			
00004D30				4294	VRI_B	VGM 0, 25, 3	
00004D30		00004D30		4295+	DS	0FD	
00004D30	00004D78			4296+	USING	*, R5	base for test data and test routine
00004D34	008B			4297+T139	DC	A(X139)	address of test routine
00004D36	00			4298+	DC	H' 139'	test number
00004D37	03			4299+	DC	X' 00'	
00004D38	00			4300+	DC	HL1' 3'	M4 field
00004D39	19			4301+	DC	HL1' 0'	i2 used
00004D3A	E5C7D440 40404040			4302+	DC	HL1' 25'	i3 used
00004D44	00004D9C			4303+	DC	CL8' VGM	instruction name
00004D48	00004DAC			4304+	DC	A(RE139+16)	address of v2 source
00004D4C	00000010			4305+	DC	A(RE139+32)	address of v3 source
00004D50	00004D8C			4306+	DC	A(16)	result length
00004D58	00000000 00000000			4307+REA139	DC	A(RE139)	result address
00004D60	00000000 00000000			4308+	DS	FD	gap
				4309+V10139	DS	XL16	V1 output

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00004D68	00000000 00000000						
00004D70	00000000 00000000			4310+	DS	FD	gap
				4311+*			
00004D78				4312+X139	DS	0F	
00004D78	E760 8EAC 0806		000010AC	4313+	VL	V22, V1FUDGE	
00004D7E	E760 0019 3846			4314+	VGM	V22, 0, 25, 3	test instruction (dest is a source)
00004D84	E760 5030 080E		00004D60	4315+	VST	V22, V10139	save v1 output
00004D8A	07FB			4316+	BR	R11	return
00004D8C				4317+RE139	DC	0F	xl16 expected result
00004D8C				4318+	DROP	R5	
00004D8C	FFFFFFFFC0 00000000			4319	DC	XL16' FFFFFFFC000000000 FFFFFFFC000000000'	result t
00004D94	FFFFFFFFC0 00000000						
				4320			
				4321	VRI_B	VGM 0, 30, 3	
00004DA0				4322+	DS	0FD	
00004DA0		00004DA0		4323+	USING	*, R5	base for test data and test routine
00004DA0	00004DE8			4324+T140	DC	A(X140)	address of test routine
00004DA4	008C			4325+	DC	H' 140'	test number
00004DA6	00			4326+	DC	X' 00'	
00004DA7	03			4327+	DC	HL1' 3'	M4 field
00004DA8	00			4328+	DC	HL1' 0'	i2 used
00004DA9	1E			4329+	DC	HL1' 30'	i3 used
00004DAA	E5C7D440 40404040			4330+	DC	CL8' VGM	instruction name
00004DB4	00004E0C			4331+	DC	A(RE140+16)	address of v2 source
00004DB8	00004E1C			4332+	DC	A(RE140+32)	address of v3 source
00004DBC	00000010			4333+	DC	A(16)	result length
00004DC0	00004DFC			4334+REA140	DC	A(RE140)	result address
00004DC8	00000000 00000000			4335+	DS	FD	gap
00004DD0	00000000 00000000			4336+V10140	DS	XL16	V1 output
00004DD8	00000000 00000000						
00004DE0	00000000 00000000			4337+	DS	FD	gap
				4338+*			
00004DE8				4339+X140	DS	0F	
00004DE8	E760 8EAC 0806		000010AC	4340+	VL	V22, V1FUDGE	
00004DEE	E760 001E 3846			4341+	VGM	V22, 0, 30, 3	test instruction (dest is a source)
00004DF4	E760 5030 080E		00004DD0	4342+	VST	V22, V10140	save v1 output
00004DFA	07FB			4343+	BR	R11	return
00004DFC				4344+RE140	DC	0F	xl16 expected result
00004DFC				4345+	DROP	R5	
00004DFC	FFFFFFFFFE 00000000			4346	DC	XL16' FFFFFFFFE00000000 FFFFFFFFE00000000'	result t
00004E04	FFFFFFFFFE 00000000						
				4347			
				4348	VRI_B	VGM 0, 31, 3	
00004E10				4349+	DS	0FD	
00004E10		00004E10		4350+	USING	*, R5	base for test data and test routine
00004E10	00004E58			4351+T141	DC	A(X141)	address of test routine
00004E14	008D			4352+	DC	H' 141'	test number
00004E16	00			4353+	DC	X' 00'	
00004E17	03			4354+	DC	HL1' 3'	M4 field
00004E18	00			4355+	DC	HL1' 0'	i2 used
00004E19	1F			4356+	DC	HL1' 31'	i3 used
00004E1A	E5C7D440 40404040			4357+	DC	CL8' VGM	instruction name
00004E24	00004E7C			4358+	DC	A(RE141+16)	address of v2 source
00004E28	00004E8C			4359+	DC	A(RE141+32)	address of v3 source
00004E2C	00000010			4360+	DC	A(16)	result length
00004E30	00004E6C			4361+REA141	DC	A(RE141)	result address

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00004E38	00000000 00000000			4362+	DS	FD	gap
00004E40	00000000 00000000			4363+V10141	DS	XL16	V1 output
00004E48	00000000 00000000						
00004E50	00000000 00000000			4364+	DS	FD	gap
				4365+*			
00004E58				4366+X141	DS	OF	
00004E58	E760 8EAC 0806		000010AC	4367+	VL	V22, V1FUDGE	
00004E5E	E760 001F 3846			4368+	VGM	V22, 0, 31, 3	test instruction (dest is a source)
00004E64	E760 5030 080E		00004E40	4369+	VST	V22, V10141	save v1 output
00004E6A	07FB			4370+	BR	R11	return
00004E6C				4371+RE141	DC	OF	xl16 expected result
00004E6C				4372+	DROP	R5	
00004E6C	FFFFFFFF 00000000			4373	DC	XL16' FFFFFFFFFF00000000 FFFFFFFFFF00000000'	result
00004E74	FFFFFFFF 00000000						
				4374			
				4375	VRI_B	VGM 0, 32, 3	
00004E80				4376+	DS	OFD	
00004E80		00004E80		4377+	USING	*, R5	base for test data and test routine
00004E80	00004EC8			4378+T142	DC	A(X142)	address of test routine
00004E84	008E			4379+	DC	H' 142'	test number
00004E86	00			4380+	DC	X' 00'	
00004E87	03			4381+	DC	HL1' 3'	M4 field
00004E88	00			4382+	DC	HL1' 0'	i2 used
00004E89	20			4383+	DC	HL1' 32'	i3 used
00004E8A	E5C7D440 40404040			4384+	DC	CL8' VGM	instruction name
00004E94	00004EEC			4385+	DC	A(RE142+16)	address of v2 source
00004E98	00004EFC			4386+	DC	A(RE142+32)	address of v3 source
00004E9C	00000010			4387+	DC	A(16)	result length
00004EA0	00004EDC			4388+REA142	DC	A(RE142)	result address
00004EA8	00000000 00000000			4389+	DS	FD	gap
00004EB0	00000000 00000000			4390+V10142	DS	XL16	V1 output
00004EB8	00000000 00000000						
00004EC0	00000000 00000000			4391+	DS	FD	gap
				4392+*			
00004EC8				4393+X142	DS	OF	
00004EC8	E760 8EAC 0806		000010AC	4394+	VL	V22, V1FUDGE	
00004ECE	E760 0020 3846			4395+	VGM	V22, 0, 32, 3	test instruction (dest is a source)
00004ED4	E760 5030 080E		00004EB0	4396+	VST	V22, V10142	save v1 output
00004EDA	07FB			4397+	BR	R11	return
00004EDC				4398+RE142	DC	OF	xl16 expected result
00004EDC				4399+	DROP	R5	
00004EDC	FFFFFFFF 80000000			4400	DC	XL16' FFFFFFFFFF80000000 FFFFFFFFFF80000000'	result
00004EE4	FFFFFFFF 80000000						
				4401			
				4402	VRI_B	VGM 0, 33, 3	
00004EF0				4403+	DS	OFD	
00004EF0		00004EF0		4404+	USING	*, R5	base for test data and test routine
00004EF0	00004F38			4405+T143	DC	A(X143)	address of test routine
00004EF4	008F			4406+	DC	H' 143'	test number
00004EF6	00			4407+	DC	X' 00'	
00004EF7	03			4408+	DC	HL1' 3'	M4 field
00004EF8	00			4409+	DC	HL1' 0'	i2 used
00004EF9	21			4410+	DC	HL1' 33'	i3 used
00004EFA	E5C7D440 40404040			4411+	DC	CL8' VGM	instruction name
00004F04	00004F5C			4412+	DC	A(RE143+16)	address of v2 source
00004F08	00004F6C			4413+	DC	A(RE143+32)	address of v3 source



LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00004F0C	00000010			4414+	DC	A(16)	result length
00004F10	00004F4C			4415+REA143	DC	A(RE143)	result address
00004F18	00000000 00000000			4416+	DS	FD	gap
00004F20	00000000 00000000			4417+V10143	DS	XL16	V1 output
00004F28	00000000 00000000						
00004F30	00000000 00000000			4418+	DS	FD	gap
				4419+*			
00004F38				4420+X143	DS	0F	
00004F38	E760 8EAC 0806		000010AC	4421+	VL	V22, V1FUDGE	
00004F3E	E760 0021 3846			4422+	VGM	V22, 0, 33, 3	test instruction (dest is a source)
00004F44	E760 5030 080E		00004F20	4423+	VST	V22, V10143	save v1 output
00004F4A	07FB			4424+	BR	R11	return
00004F4C				4425+RE143	DC	0F	xl16 expected result
00004F4C				4426+	DROP	R5	
00004F4C	FFFFFFFF C0000000			4427	DC	XL16' FFFFFFFFC0000000 FFFFFFFFC0000000'	result
00004F54	FFFFFFFF C0000000						
				4428			
00004F60				4429	VRI_B	VGM 0, 55, 3	
00004F60		00004F60		4430+	DS	0FD	
00004F60	00004FA8			4431+	USING	*, R5	base for test data and test routine
00004F64	0090			4432+T144	DC	A(X144)	address of test routine
00004F66	00			4433+	DC	H' 144'	test number
00004F66	00			4434+	DC	X' 00'	
00004F67	03			4435+	DC	HL1' 3'	M4 field
00004F68	00			4436+	DC	HL1' 0'	i2 used
00004F69	37			4437+	DC	HL1' 55'	i3 used
00004F6A	E5C7D440 40404040			4438+	DC	CL8' VGM	instruction name
00004F74	00004FCC			4439+	DC	A(RE144+16)	address of v2 source
00004F78	00004FDC			4440+	DC	A(RE144+32)	address of v3 source
00004F7C	00000010			4441+	DC	A(16)	result length
00004F80	00004FBC			4442+REA144	DC	A(RE144)	result address
00004F88	00000000 00000000			4443+	DS	FD	gap
00004F90	00000000 00000000			4444+V10144	DS	XL16	V1 output
00004F98	00000000 00000000						
00004FA0	00000000 00000000			4445+	DS	FD	gap
				4446+*			
00004FA8				4447+X144	DS	0F	
00004FA8	E760 8EAC 0806		000010AC	4448+	VL	V22, V1FUDGE	
00004FAE	E760 0037 3846			4449+	VGM	V22, 0, 55, 3	test instruction (dest is a source)
00004FB4	E760 5030 080E		00004F90	4450+	VST	V22, V10144	save v1 output
00004FBA	07FB			4451+	BR	R11	return
00004FBC				4452+RE144	DC	0F	xl16 expected result
00004FBC				4453+	DROP	R5	
00004FBC	FFFFFFFF FFFFFFF00			4454	DC	XL16' FFFFFFFFFFFFFFFF00 FFFFFFFFFFFFFFFF00'	result
00004FC4	FFFFFFFF FFFFFFF00						
				4455			
00004FD0				4456	VRI_B	VGM 0, 64, 3	
00004FD0		00004FD0		4457+	DS	0FD	
00004FD0	00005018			4458+	USING	*, R5	base for test data and test routine
00004FD4	0091			4459+T145	DC	A(X145)	address of test routine
00004FD6	00			4460+	DC	H' 145'	test number
00004FD6	00			4461+	DC	X' 00'	
00004FD7	03			4462+	DC	HL1' 3'	M4 field
00004FD8	00			4463+	DC	HL1' 0'	i2 used
00004FD9	40			4464+	DC	HL1' 64'	i3 used
00004FDA	E5C7D440 40404040			4465+	DC	CL8' VGM	instruction name





LOC	OBJECT CODE	ADDR1	ADDR2	STMT	
				4484 *Doubleword: I2<I3; I2=1	
				4485 VRI_B VGM 1, 1, 3	
00005040				4486+ DS OFD	
00005040		00005040		4487+ USING *, R5	base for test data and test routine
00005040	00005088			4488+T146 DC A(X146)	address of test routine
00005044	0092			4489+ DC H' 146'	test number
00005046	00			4490+ DC X' 00'	
00005047	03			4491+ DC HL1' 3'	M4 field
00005048	01			4492+ DC HL1' 1'	i2 used
00005049	01			4493+ DC HL1' 1'	i3 used
0000504A	E5C7D440 40404040			4494+ DC CL8' VGM	instruction name
00005054	000050AC			4495+ DC A(RE146+16)	address of v2 source
00005058	000050BC			4496+ DC A(RE146+32)	address of v3 source
0000505C	00000010			4497+ DC A(16)	result length
00005060	0000509C			4498+REA146 DC A(RE146)	result address
00005068	00000000 00000000			4499+ DS FD	gap
00005070	00000000 00000000			4500+V10146 DS XL16	V1 output
00005078	00000000 00000000				
00005080	00000000 00000000			4501+ DS FD	gap
				4502+*	
00005088				4503+X146 DS OF	
00005088	E760 8EAC 0806		000010AC	4504+ VL V22, V1FUDGE	
0000508E	E760 0101 3846			4505+ VGM V22, 1, 1, 3	test instruction (dest is a source)
00005094	E760 5030 080E		00005070	4506+ VST V22, V10146	save v1 output
0000509A	07FB			4507+ BR R11	return
0000509C				4508+RE146 DC OF	xl16 expected result
0000509C				4509+ DROP R5	
0000509C	40000000 00000000			4510 DC XL16' 4000000000000000 4000000000000000'	result t
000050A4	40000000 00000000				
				4511	
				4512 VRI_B VGM 1, 2, 3	
000050B0				4513+ DS OFD	
000050B0		000050B0		4514+ USING *, R5	base for test data and test routine
000050B0	000050F8			4515+T147 DC A(X147)	address of test routine
000050B4	0093			4516+ DC H' 147'	test number
000050B6	00			4517+ DC X' 00'	
000050B7	03			4518+ DC HL1' 3'	M4 field
000050B8	01			4519+ DC HL1' 1'	i2 used
000050B9	02			4520+ DC HL1' 2'	i3 used
000050BA	E5C7D440 40404040			4521+ DC CL8' VGM	instruction name
000050C4	0000511C			4522+ DC A(RE147+16)	address of v2 source
000050C8	0000512C			4523+ DC A(RE147+32)	address of v3 source
000050CC	00000010			4524+ DC A(16)	result length
000050D0	0000510C			4525+REA147 DC A(RE147)	result address
000050D8	00000000 00000000			4526+ DS FD	gap
000050E0	00000000 00000000			4527+V10147 DS XL16	V1 output
000050E8	00000000 00000000				
000050F0	00000000 00000000			4528+ DS FD	gap
				4529+*	
000050F8				4530+X147 DS OF	
000050F8	E760 8EAC 0806		000010AC	4531+ VL V22, V1FUDGE	
000050FE	E760 0102 3846			4532+ VGM V22, 1, 2, 3	test instruction (dest is a source)
00005104	E760 5030 080E		000050E0	4533+ VST V22, V10147	save v1 output
0000510A	07FB			4534+ BR R11	return
0000510C				4535+RE147 DC OF	xl16 expected result
0000510C				4536+ DROP R5	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
0000510C	60000000 00000000			4537	DC	XL16' 600000000000000000 600000000000000000'	result
00005114	60000000 00000000						
				4538			
				4539	VRI_B	VGM 1, 4, 3	
00005120				4540+	DS	OFD	
00005120		00005120		4541+	USING	*, R5	base for test data and test routine
00005120	00005168			4542+T148	DC	A(X148)	address of test routine
00005124	0094			4543+	DC	H' 148'	test number
00005126	00			4544+	DC	X' 00'	
00005127	03			4545+	DC	HL1' 3'	M4 field
00005128	01			4546+	DC	HL1' 1'	i2 used
00005129	04			4547+	DC	HL1' 4'	i3 used
0000512A	E5C7D440 40404040			4548+	DC	CL8' VGM	instruction name
00005134	0000518C			4549+	DC	A(RE148+16)	address of v2 source
00005138	0000519C			4550+	DC	A(RE148+32)	address of v3 source
0000513C	00000010			4551+	DC	A(16)	result length
00005140	0000517C			4552+REA148	DC	A(RE148)	result address
00005148	00000000 00000000			4553+	DS	FD	gap
00005150	00000000 00000000			4554+V10148	DS	XL16	V1 output
00005158	00000000 00000000						
00005160	00000000 00000000			4555+	DS	FD	gap
				4556+*			
00005168				4557+X148	DS	OF	
00005168	E760 8EAC 0806		000010AC	4558+	VL	V22, V1FUDGE	
0000516E	E760 0104 3846			4559+	VGM	V22, 1, 4, 3	test instruction (dest is a source)
00005174	E760 5030 080E		00005150	4560+	VST	V22, V10148	save v1 output
0000517A	07FB			4561+	BR	R11	return
0000517C				4562+RE148	DC	OF	xl16 expected result
0000517C				4563+	DROP	R5	
0000517C	78000000 00000000			4564	DC	XL16' 780000000000000000 780000000000000000'	result
00005184	78000000 00000000						
				4565			
				4566	VRI_B	VGM 1, 7, 3	
00005190				4567+	DS	OFD	
00005190		00005190		4568+	USING	*, R5	base for test data and test routine
00005190	000051D8			4569+T149	DC	A(X149)	address of test routine
00005194	0095			4570+	DC	H' 149'	test number
00005196	00			4571+	DC	X' 00'	
00005197	03			4572+	DC	HL1' 3'	M4 field
00005198	01			4573+	DC	HL1' 1'	i2 used
00005199	07			4574+	DC	HL1' 7'	i3 used
0000519A	E5C7D440 40404040			4575+	DC	CL8' VGM	instruction name
000051A4	000051FC			4576+	DC	A(RE149+16)	address of v2 source
000051A8	0000520C			4577+	DC	A(RE149+32)	address of v3 source
000051AC	00000010			4578+	DC	A(16)	result length
000051B0	000051EC			4579+REA149	DC	A(RE149)	result address
000051B8	00000000 00000000			4580+	DS	FD	gap
000051C0	00000000 00000000			4581+V10149	DS	XL16	V1 output
000051C8	00000000 00000000						
000051D0	00000000 00000000			4582+	DS	FD	gap
				4583+*			
000051D8				4584+X149	DS	OF	
000051D8	E760 8EAC 0806		000010AC	4585+	VL	V22, V1FUDGE	
000051DE	E760 0107 3846			4586+	VGM	V22, 1, 7, 3	test instruction (dest is a source)
000051E4	E760 5030 080E		000051C0	4587+	VST	V22, V10149	save v1 output
000051EA	07FB			4588+	BR	R11	return

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
000051EC				4589+RE149	DC	0F	xl16 expected result
000051EC				4590+	DROP	R5	
000051EC	7F000000 00000000			4591	DC	XL16' 7F00000000000000 7F00000000000000'	result
000051F4	7F000000 00000000						
				4592			
				4593	VRI_B	VGM 1, 8, 3	
00005200				4594+	DS	0FD	
00005200		00005200		4595+	USING	*, R5	base for test data and test routine
00005200	00005248			4596+T150	DC	A(X150)	address of test routine
00005204	0096			4597+	DC	H' 150'	test number
00005206	00			4598+	DC	X' 00'	
00005207	03			4599+	DC	HL1' 3'	M4 field
00005208	01			4600+	DC	HL1' 1'	i2 used
00005209	08			4601+	DC	HL1' 8'	i3 used
0000520A	E5C7D440 40404040			4602+	DC	CL8' VGM	instruction name
00005214	0000526C			4603+	DC	A(RE150+16)	address of v2 source
00005218	0000527C			4604+	DC	A(RE150+32)	address of v3 source
0000521C	00000010			4605+	DC	A(16)	result length
00005220	0000525C			4606+REA150	DC	A(RE150)	result address
00005228	00000000 00000000			4607+	DS	FD	gap
00005230	00000000 00000000			4608+V10150	DS	XL16	V1 output
00005238	00000000 00000000						
00005240	00000000 00000000			4609+	DS	FD	gap
				4610+*			
00005248				4611+X150	DS	0F	
00005248	E760 8EAC 0806		000010AC	4612+	VL	V22, V1FUDGE	
0000524E	E760 0108 3846			4613+	VGM	V22, 1, 8, 3	test instruction (dest is a source)
00005254	E760 5030 080E		00005230	4614+	VST	V22, V10150	save v1 output
0000525A	07FB			4615+	BR	R11	return
0000525C				4616+RE150	DC	0F	xl16 expected result
0000525C				4617+	DROP	R5	
0000525C	7F800000 00000000			4618	DC	XL16' 7F80000000000000 7F80000000000000'	result
00005264	7F800000 00000000						
				4619			
				4620	VRI_B	VGM 1, 9, 3	
00005270				4621+	DS	0FD	
00005270		00005270		4622+	USING	*, R5	base for test data and test routine
00005270	000052B8			4623+T151	DC	A(X151)	address of test routine
00005274	0097			4624+	DC	H' 151'	test number
00005276	00			4625+	DC	X' 00'	
00005277	03			4626+	DC	HL1' 3'	M4 field
00005278	01			4627+	DC	HL1' 1'	i2 used
00005279	09			4628+	DC	HL1' 9'	i3 used
0000527A	E5C7D440 40404040			4629+	DC	CL8' VGM	instruction name
00005284	000052DC			4630+	DC	A(RE151+16)	address of v2 source
00005288	000052EC			4631+	DC	A(RE151+32)	address of v3 source
0000528C	00000010			4632+	DC	A(16)	result length
00005290	000052CC			4633+REA151	DC	A(RE151)	result address
00005298	00000000 00000000			4634+	DS	FD	gap
000052A0	00000000 00000000			4635+V10151	DS	XL16	V1 output
000052A8	00000000 00000000						
000052B0	00000000 00000000			4636+	DS	FD	gap
				4637+*			
000052B8				4638+X151	DS	0F	
000052B8	E760 8EAC 0806		000010AC	4639+	VL	V22, V1FUDGE	
000052BE	E760 0109 3846			4640+	VGM	V22, 1, 9, 3	test instruction (dest is a source)

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
000052C4	E760 5030 080E		000052A0	4641+	VST	V22, V10151	save v1 output
000052CA	07FB			4642+	BR	R11	return
000052CC				4643+RE151	DC	0F	xl16 expected result
000052CC				4644+	DROP	R5	
000052CC	7FC00000 00000000			4645	DC	XL16' 7FC0000000000000 7FC0000000000000'	result t
000052D4	7FC00000 00000000						
				4646			
				4647	VRI_B	VGM 1, 13, 3	
000052E0				4648+	DS	0FD	
000052E0		000052E0		4649+	USING	*, R5	base for test data and test routine
000052E0	00005328			4650+T152	DC	A(X152)	address of test routine
000052E4	0098			4651+	DC	H' 152'	test number
000052E6	00			4652+	DC	X' 00'	
000052E7	03			4653+	DC	HL1' 3'	M4 field
000052E8	01			4654+	DC	HL1' 1'	i2 used
000052E9	0D			4655+	DC	HL1' 13'	i3 used
000052EA	E5C7D440 40404040			4656+	DC	CL8' VGM	instruction name
000052F4	0000534C			4657+	DC	A(RE152+16)	address of v2 source
000052F8	0000535C			4658+	DC	A(RE152+32)	address of v3 source
000052FC	00000010			4659+	DC	A(16)	result length
00005300	0000533C			4660+REA152	DC	A(RE152)	result address
00005308	00000000 00000000			4661+	DS	FD	gap
00005310	00000000 00000000			4662+V10152	DS	XL16	V1 output
00005318	00000000 00000000						
00005320	00000000 00000000			4663+	DS	FD	gap
				4664+*			
00005328				4665+X152	DS	0F	
00005328	E760 8EAC 0806		000010AC	4666+	VL	V22, V1FUDGE	
0000532E	E760 010D 3846			4667+	VGM	V22, 1, 13, 3	test instruction (dest is a source)
00005334	E760 5030 080E		00005310	4668+	VST	V22, V10152	save v1 output
0000533A	07FB			4669+	BR	R11	return
0000533C				4670+RE152	DC	0F	xl16 expected result
0000533C				4671+	DROP	R5	
0000533C	7FFC0000 00000000			4672	DC	XL16' 7FFC000000000000 7FFC000000000000'	result t
00005344	7FFC0000 00000000						
				4673			
				4674	VRI_B	VGM 1, 15, 3	
00005350				4675+	DS	0FD	
00005350		00005350		4676+	USING	*, R5	base for test data and test routine
00005350	00005398			4677+T153	DC	A(X153)	address of test routine
00005354	0099			4678+	DC	H' 153'	test number
00005356	00			4679+	DC	X' 00'	
00005357	03			4680+	DC	HL1' 3'	M4 field
00005358	01			4681+	DC	HL1' 1'	i2 used
00005359	0F			4682+	DC	HL1' 15'	i3 used
0000535A	E5C7D440 40404040			4683+	DC	CL8' VGM	instruction name
00005364	000053BC			4684+	DC	A(RE153+16)	address of v2 source
00005368	000053CC			4685+	DC	A(RE153+32)	address of v3 source
0000536C	00000010			4686+	DC	A(16)	result length
00005370	000053AC			4687+REA153	DC	A(RE153)	result address
00005378	00000000 00000000			4688+	DS	FD	gap
00005380	00000000 00000000			4689+V10153	DS	XL16	V1 output
00005388	00000000 00000000						
00005390	00000000 00000000			4690+	DS	FD	gap
				4691+*			
00005398				4692+X153	DS	0F	



LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00005398	E760 8EAC 0806		000010AC	4693+	VL	V22, V1FUDGE	
0000539E	E760 010F 3846			4694+	VGM	V22, 1, 15, 3	test instruction (dest is a source)
000053A4	E760 5030 080E		00005380	4695+	VST	V22, V10153	save v1 output
000053AA	07FB			4696+	BR	R11	return
000053AC				4697+RE153	DC	0F	xl16 expected result
000053AC				4698+	DROP	R5	
000053AC	7FFF0000 00000000			4699	DC	XL16' 7FFF000000000000 7FFF000000000000'	result
000053B4	7FFF0000 00000000						
				4700			
				4701	VRI_B	VGM 1, 16, 3	
000053C0				4702+	DS	0FD	
000053C0		000053C0		4703+	USING	*, R5	base for test data and test routine
000053C0	00005408			4704+T154	DC	A(X154)	address of test routine
000053C4	009A			4705+	DC	H' 154'	test number
000053C6	00			4706+	DC	X' 00'	
000053C7	03			4707+	DC	HL1' 3'	M4 field
000053C8	01			4708+	DC	HL1' 1'	i2 used
000053C9	10			4709+	DC	HL1' 16'	i3 used
000053CA	E5C7D440 40404040			4710+	DC	CL8' VGM	instruction name
000053D4	0000542C			4711+	DC	A(RE154+16)	address of v2 source
000053D8	0000543C			4712+	DC	A(RE154+32)	address of v3 source
000053DC	00000010			4713+	DC	A(16)	result length
000053E0	0000541C			4714+REA154	DC	A(RE154)	result address
000053E8	00000000 00000000			4715+	DS	FD	gap
000053F0	00000000 00000000			4716+V10154	DS	XL16	V1 output
000053F8	00000000 00000000						
00005400	00000000 00000000			4717+	DS	FD	gap
				4718+*			
00005408				4719+X154	DS	0F	
00005408	E760 8EAC 0806		000010AC	4720+	VL	V22, V1FUDGE	
0000540E	E760 0110 3846			4721+	VGM	V22, 1, 16, 3	test instruction (dest is a source)
00005414	E760 5030 080E		000053F0	4722+	VST	V22, V10154	save v1 output
0000541A	07FB			4723+	BR	R11	return
0000541C				4724+RE154	DC	0F	xl16 expected result
0000541C				4725+	DROP	R5	
0000541C	7FFF8000 00000000			4726	DC	XL16' 7FFF800000000000 7FFF800000000000'	result
00005424	7FFF8000 00000000						
				4727			
				4728	VRI_B	VGM 1, 17, 3	
00005430				4729+	DS	0FD	
00005430		00005430		4730+	USING	*, R5	base for test data and test routine
00005430	00005478			4731+T155	DC	A(X155)	address of test routine
00005434	009B			4732+	DC	H' 155'	test number
00005436	00			4733+	DC	X' 00'	
00005437	03			4734+	DC	HL1' 3'	M4 field
00005438	01			4735+	DC	HL1' 1'	i2 used
00005439	11			4736+	DC	HL1' 17'	i3 used
0000543A	E5C7D440 40404040			4737+	DC	CL8' VGM	instruction name
00005444	0000549C			4738+	DC	A(RE155+16)	address of v2 source
00005448	000054AC			4739+	DC	A(RE155+32)	address of v3 source
0000544C	00000010			4740+	DC	A(16)	result length
00005450	0000548C			4741+REA155	DC	A(RE155)	result address
00005458	00000000 00000000			4742+	DS	FD	gap
00005460	00000000 00000000			4743+V10155	DS	XL16	V1 output
00005468	00000000 00000000						
00005470	00000000 00000000			4744+	DS	FD	gap

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00005478				4745+*			
00005478	E760 8EAC 0806		000010AC	4746+X155	DS	0F	
0000547E	E760 0111 3846			4747+	VL	V22, V1FUDGE	
00005484	E760 5030 080E		00005460	4748+	VGM	V22, 1, 17, 3	test instruction (dest is a source)
0000548A	07FB			4749+	VST	V22, V10155	save v1 output
0000548C				4750+	BR	R11	return
0000548C				4751+RE155	DC	0F	xl16 expected result
0000548C				4752+	DROP	R5	
0000548C	7FFFC000 00000000			4753	DC	XL16' 7FFFC00000000000 7FFFC00000000000'	result
00005494	7FFFC000 00000000						
000054A0				4754			
000054A0		000054A0		4755	VRI_B	VGM 1, 25, 3	
000054A0	000054E8			4756+	DS	0FD	
000054A4	009C			4757+	USING	*, R5	base for test data and test routine
000054A6	00			4758+T156	DC	A(X156)	address of test routine
000054A7	03			4759+	DC	H' 156'	test number
000054A8	01			4760+	DC	X' 00'	
000054A9	19			4761+	DC	HL1' 3'	M4 field
000054AA	E5C7D440 40404040			4762+	DC	HL1' 1'	i2 used
000054B4	0000550C			4763+	DC	HL1' 25'	i3 used
000054B8	0000551C			4764+	DC	CL8' VGM	instruction name
000054BC	00000010			4765+	DC	A(RE156+16)	address of v2 source
000054C0	000054FC			4766+	DC	A(RE156+32)	address of v3 source
000054C8	00000000 00000000			4767+	DC	A(16)	result length
000054D0	00000000 00000000			4768+REA156	DC	A(RE156)	result address
000054D8	00000000 00000000			4769+	DS	FD	gap
000054E0	00000000 00000000			4770+V10156	DS	XL16	V1 output
000054E8				4771+	DS	FD	gap
000054E8	E760 8EAC 0806		000010AC	4772+*			
000054EE	E760 0119 3846			4773+X156	DS	0F	
000054F4	E760 5030 080E		000054D0	4774+	VL	V22, V1FUDGE	
000054FA	07FB			4775+	VGM	V22, 1, 25, 3	test instruction (dest is a source)
000054FC				4776+	VST	V22, V10156	save v1 output
000054FC				4777+	BR	R11	return
000054FC				4778+RE156	DC	0F	xl16 expected result
000054FC	7FFFFFFC0 00000000			4779+	DROP	R5	
00005504	7FFFFFFC0 00000000			4780	DC	XL16' 7FFFFFFC000000000 7FFFFFFC000000000'	result
00005510				4781			
00005510		00005510		4782	VRI_B	VGM 1, 30, 3	
00005510	00005558			4783+	DS	0FD	
00005514	009D			4784+	USING	*, R5	base for test data and test routine
00005516	00			4785+T157	DC	A(X157)	address of test routine
00005517	03			4786+	DC	H' 157'	test number
00005518	01			4787+	DC	X' 00'	
00005519	1E			4788+	DC	HL1' 3'	M4 field
0000551A	E5C7D440 40404040			4789+	DC	HL1' 1'	i2 used
00005524	0000557C			4790+	DC	HL1' 30'	i3 used
00005528	0000558C			4791+	DC	CL8' VGM	instruction name
0000552C	00000010			4792+	DC	A(RE157+16)	address of v2 source
00005530	0000556C			4793+	DC	A(RE157+32)	address of v3 source
00005538	00000000 00000000			4794+	DC	A(16)	result length
00005540	00000000 00000000			4795+REA157	DC	A(RE157)	result address
				4796+	DS	FD	gap
				4797+V10157	DS	XL16	V1 output

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00005548	00000000 00000000						
00005550	00000000 00000000			4798+	DS	FD	gap
				4799+*			
00005558				4800+X157	DS	OF	
00005558	E760 8EAC 0806		000010AC	4801+	VL	V22, V1FUDGE	
0000555E	E760 011E 3846			4802+	VGM	V22, 1, 30, 3	test instruction (dest is a source)
00005564	E760 5030 080E		00005540	4803+	VST	V22, V10157	save v1 output
0000556A	07FB			4804+	BR	R11	return
0000556C				4805+RE157	DC	OF	xl16 expected result
0000556C				4806+	DROP	R5	
0000556C	7FFFFFFE 00000000			4807	DC	XL16' 7FFFFFFE00000000 7FFFFFFE00000000'	result t
00005574	7FFFFFFE 00000000						
				4808			
				4809	VRI_B	VGM 1, 31, 3	
00005580				4810+	DS	OFD	
00005580		00005580		4811+	USING	*, R5	base for test data and test routine
00005580	000055C8			4812+T158	DC	A(X158)	address of test routine
00005584	009E			4813+	DC	H' 158'	test number
00005586	00			4814+	DC	X' 00'	
00005587	03			4815+	DC	HL1' 3'	M4 field
00005588	01			4816+	DC	HL1' 1'	i2 used
00005589	1F			4817+	DC	HL1' 31'	i3 used
0000558A	E5C7D440 40404040			4818+	DC	CL8' VGM	instruction name
00005594	000055EC			4819+	DC	A(RE158+16)	address of v2 source
00005598	000055FC			4820+	DC	A(RE158+32)	address of v3 source
0000559C	00000010			4821+	DC	A(16)	result length
000055A0	000055DC			4822+REA158	DC	A(RE158)	result address
000055A8	00000000 00000000			4823+	DS	FD	gap
000055B0	00000000 00000000			4824+V10158	DS	XL16	V1 output
000055B8	00000000 00000000						
000055C0	00000000 00000000			4825+	DS	FD	gap
				4826+*			
000055C8				4827+X158	DS	OF	
000055C8	E760 8EAC 0806		000010AC	4828+	VL	V22, V1FUDGE	
000055CE	E760 011F 3846			4829+	VGM	V22, 1, 31, 3	test instruction (dest is a source)
000055D4	E760 5030 080E		000055B0	4830+	VST	V22, V10158	save v1 output
000055DA	07FB			4831+	BR	R11	return
000055DC				4832+RE158	DC	OF	xl16 expected result
000055DC				4833+	DROP	R5	
000055DC	7FFFFFFF 00000000			4834	DC	XL16' 7FFFFFFF00000000 7FFFFFFF00000000'	result t
000055E4	7FFFFFFF 00000000						
				4835			
				4836	VRI_B	VGM 1, 32, 3	
000055F0				4837+	DS	OFD	
000055F0		000055F0		4838+	USING	*, R5	base for test data and test routine
000055F0	00005638			4839+T159	DC	A(X159)	address of test routine
000055F4	009F			4840+	DC	H' 159'	test number
000055F6	00			4841+	DC	X' 00'	
000055F7	03			4842+	DC	HL1' 3'	M4 field
000055F8	01			4843+	DC	HL1' 1'	i2 used
000055F9	20			4844+	DC	HL1' 32'	i3 used
000055FA	E5C7D440 40404040			4845+	DC	CL8' VGM	instruction name
00005604	0000565C			4846+	DC	A(RE159+16)	address of v2 source
00005608	0000566C			4847+	DC	A(RE159+32)	address of v3 source
0000560C	00000010			4848+	DC	A(16)	result length
00005610	0000564C			4849+REA159	DC	A(RE159)	result address

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00005618	00000000 00000000			4850+	DS	FD	gap
00005620	00000000 00000000			4851+V10159	DS	XL16	V1 output
00005628	00000000 00000000						
00005630	00000000 00000000			4852+	DS	FD	gap
				4853+*			
00005638				4854+X159	DS	OF	
00005638	E760 8EAC 0806		000010AC	4855+	VL	V22, V1FUDGE	
0000563E	E760 0120 3846			4856+	VGM	V22, 1, 32, 3	test instruction (dest is a source)
00005644	E760 5030 080E		00005620	4857+	VST	V22, V10159	save v1 output
0000564A	07FB			4858+	BR	R11	return
0000564C				4859+RE159	DC	OF	xl16 expected result
0000564C				4860+	DROP	R5	
0000564C	7FFFFFFF 80000000			4861	DC	XL16' 7FFFFFFF80000000 7FFFFFFF80000000'	result
00005654	7FFFFFFF 80000000						
				4862			
				4863	VRI_B	VGM 1, 33, 3	
00005660				4864+	DS	OFD	
00005660		00005660		4865+	USING	*, R5	base for test data and test routine
00005660	000056A8			4866+T160	DC	A(X160)	address of test routine
00005664	00A0			4867+	DC	H' 160'	test number
00005666	00			4868+	DC	X' 00'	
00005667	03			4869+	DC	HL1' 3'	M4 field
00005668	01			4870+	DC	HL1' 1'	i2 used
00005669	21			4871+	DC	HL1' 33'	i3 used
0000566A	E5C7D440 40404040			4872+	DC	CL8' VGM	instruction name
00005674	000056CC			4873+	DC	A(RE160+16)	address of v2 source
00005678	000056DC			4874+	DC	A(RE160+32)	address of v3 source
0000567C	00000010			4875+	DC	A(16)	result length
00005680	000056BC			4876+REA160	DC	A(RE160)	result address
00005688	00000000 00000000			4877+	DS	FD	gap
00005690	00000000 00000000			4878+V10160	DS	XL16	V1 output
00005698	00000000 00000000						
000056A0	00000000 00000000			4879+	DS	FD	gap
				4880+*			
000056A8				4881+X160	DS	OF	
000056A8	E760 8EAC 0806		000010AC	4882+	VL	V22, V1FUDGE	
000056AE	E760 0121 3846			4883+	VGM	V22, 1, 33, 3	test instruction (dest is a source)
000056B4	E760 5030 080E		00005690	4884+	VST	V22, V10160	save v1 output
000056BA	07FB			4885+	BR	R11	return
000056BC				4886+RE160	DC	OF	xl16 expected result
000056BC				4887+	DROP	R5	
000056BC	7FFFFFFF C0000000			4888	DC	XL16' 7FFFFFFFC0000000 7FFFFFFFC0000000'	result
000056C4	7FFFFFFF C0000000						
				4889			
				4890	VRI_B	VGM 1, 55, 3	
000056D0				4891+	DS	OFD	
000056D0		000056D0		4892+	USING	*, R5	base for test data and test routine
000056D0	00005718			4893+T161	DC	A(X161)	address of test routine
000056D4	00A1			4894+	DC	H' 161'	test number
000056D6	00			4895+	DC	X' 00'	
000056D7	03			4896+	DC	HL1' 3'	M4 field
000056D8	01			4897+	DC	HL1' 1'	i2 used
000056D9	37			4898+	DC	HL1' 55'	i3 used
000056DA	E5C7D440 40404040			4899+	DC	CL8' VGM	instruction name
000056E4	0000573C			4900+	DC	A(RE161+16)	address of v2 source
000056E8	0000574C			4901+	DC	A(RE161+32)	address of v3 source







LOC	OBJECT CODE	ADDR1	ADDR2	STMT	
				4945 *Doubleword: I2>I3; I3=0	
				4946 VRI_B VGM 1, 0, 3	
000057B0				4947+ DS OFD	
000057B0		000057B0		4948+ USING *, R5	base for test data and test routine
000057B0	000057F8			4949+T163 DC A(X163)	address of test routine
000057B4	00A3			4950+ DC H' 163'	test number
000057B6	00			4951+ DC X' 00'	
000057B7	03			4952+ DC HL1' 3'	M4 field
000057B8	01			4953+ DC HL1' 1'	i2 used
000057B9	00			4954+ DC HL1' 0'	i3 used
000057BA	E5C7D440 40404040			4955+ DC CL8' VGM	instruction name
000057C4	0000581C			4956+ DC A(RE163+16)	address of v2 source
000057C8	0000582C			4957+ DC A(RE163+32)	address of v3 source
000057CC	00000010			4958+ DC A(16)	result length
000057D0	0000580C			4959+REA163 DC A(RE163)	result address
000057D8	00000000 00000000			4960+ DS FD	gap
000057E0	00000000 00000000			4961+V10163 DS XL16	V1 output
000057E8	00000000 00000000				
000057F0	00000000 00000000			4962+ DS FD	gap
				4963+*	
000057F8				4964+X163 DS OF	
000057F8	E760 8EAC 0806	000010AC		4965+ VL V22, V1FUDGE	
000057FE	E760 0100 3846			4966+ VGM V22, 1, 0, 3	test instruction (dest is a source)
00005804	E760 5030 080E	000057E0		4967+ VST V22, V10163	save v1 output
0000580A	07FB			4968+ BR R11	return
0000580C				4969+RE163 DC OF	xl16 expected result
0000580C				4970+ DROP R5	
0000580C	FFFFFFFF FFFFFFFF			4971 DC XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF'	result t
00005814	FFFFFFFF FFFFFFFF				
				4972	
				4973 VRI_B VGM 2, 0, 3	
00005820				4974+ DS OFD	
00005820		00005820		4975+ USING *, R5	base for test data and test routine
00005820	00005868			4976+T164 DC A(X164)	address of test routine
00005824	00A4			4977+ DC H' 164'	test number
00005826	00			4978+ DC X' 00'	
00005827	03			4979+ DC HL1' 3'	M4 field
00005828	02			4980+ DC HL1' 2'	i2 used
00005829	00			4981+ DC HL1' 0'	i3 used
0000582A	E5C7D440 40404040			4982+ DC CL8' VGM	instruction name
00005834	0000588C			4983+ DC A(RE164+16)	address of v2 source
00005838	0000589C			4984+ DC A(RE164+32)	address of v3 source
0000583C	00000010			4985+ DC A(16)	result length
00005840	0000587C			4986+REA164 DC A(RE164)	result address
00005848	00000000 00000000			4987+ DS FD	gap
00005850	00000000 00000000			4988+V10164 DS XL16	V1 output
00005858	00000000 00000000				
00005860	00000000 00000000			4989+ DS FD	gap
				4990+*	
00005868				4991+X164 DS OF	
00005868	E760 8EAC 0806	000010AC		4992+ VL V22, V1FUDGE	
0000586E	E760 0200 3846			4993+ VGM V22, 2, 0, 3	test instruction (dest is a source)
00005874	E760 5030 080E	00005850		4994+ VST V22, V10164	save v1 output
0000587A	07FB			4995+ BR R11	return
0000587C				4996+RE164 DC OF	xl16 expected result
0000587C				4997+ DROP R5	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
0000587C	BFFFFFFFF FFFFFFFF			4998	DC	XL16' BFFFFFFFFFFFFFFFFF BFFFFFFFFFFFFFFFFF'	result
00005884	BFFFFFFFF FFFFFFFF						
				4999			
00005890				5000	VRI_B	VGM 4, 0, 3	
				5001+	DS	OFD	
00005890		00005890		5002+	USING	*, R5	base for test data and test routine
00005890	000058D8			5003+T165	DC	A(X165)	address of test routine
00005894	00A5			5004+	DC	H' 165'	test number
00005896	00			5005+	DC	X' 00'	
00005897	03			5006+	DC	HL1' 3'	M4 field
00005898	04			5007+	DC	HL1' 4'	i2 used
00005899	00			5008+	DC	HL1' 0'	i3 used
0000589A	E5C7D440 40404040			5009+	DC	CL8' VGM	instruction name
000058A4	000058FC			5010+	DC	A(RE165+16)	address of v2 source
000058A8	0000590C			5011+	DC	A(RE165+32)	address of v3 source
000058AC	00000010			5012+	DC	A(16)	result length
000058B0	000058EC			5013+REA165	DC	A(RE165)	result address
000058B8	00000000 00000000			5014+	DS	FD	gap
000058C0	00000000 00000000			5015+V10165	DS	XL16	V1 output
000058C8	00000000 00000000						
000058D0	00000000 00000000			5016+	DS	FD	gap
				5017+*			
000058D8				5018+X165	DS	OF	
000058D8	E760 8EAC 0806		000010AC	5019+	VL	V22, V1FUDGE	
000058DE	E760 0400 3846			5020+	VGM	V22, 4, 0, 3	test instruction (dest is a source)
000058E4	E760 5030 080E		000058C0	5021+	VST	V22, V10165	save v1 output
000058EA	07FB			5022+	BR	R11	return
000058EC				5023+RE165	DC	OF	xl16 expected result
000058EC				5024+	DROP	R5	
000058EC	8FFFFFFFF FFFFFFFF			5025	DC	XL16' 8FFFFFFFFFFFFFFFFF 8FFFFFFFFFFFFFFFFF'	result
000058F4	8FFFFFFFF FFFFFFFF						
				5026			
00005900				5027	VRI_B	VGM 6, 0, 3	
				5028+	DS	OFD	
00005900		00005900		5029+	USING	*, R5	base for test data and test routine
00005900	00005948			5030+T166	DC	A(X166)	address of test routine
00005904	00A6			5031+	DC	H' 166'	test number
00005906	00			5032+	DC	X' 00'	
00005907	03			5033+	DC	HL1' 3'	M4 field
00005908	06			5034+	DC	HL1' 6'	i2 used
00005909	00			5035+	DC	HL1' 0'	i3 used
0000590A	E5C7D440 40404040			5036+	DC	CL8' VGM	instruction name
00005914	0000596C			5037+	DC	A(RE166+16)	address of v2 source
00005918	0000597C			5038+	DC	A(RE166+32)	address of v3 source
0000591C	00000010			5039+	DC	A(16)	result length
00005920	0000595C			5040+REA166	DC	A(RE166)	result address
00005928	00000000 00000000			5041+	DS	FD	gap
00005930	00000000 00000000			5042+V10166	DS	XL16	V1 output
00005938	00000000 00000000						
00005940	00000000 00000000			5043+	DS	FD	gap
				5044+*			
00005948				5045+X166	DS	OF	
00005948	E760 8EAC 0806		000010AC	5046+	VL	V22, V1FUDGE	
0000594E	E760 0600 3846			5047+	VGM	V22, 6, 0, 3	test instruction (dest is a source)
00005954	E760 5030 080E		00005930	5048+	VST	V22, V10166	save v1 output
0000595A	07FB			5049+	BR	R11	return

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
0000595C				5050+RE166	DC	0F	xl16 expected result
0000595C				5051+	DROP	R5	
0000595C	83FFFFFF FFFFFFFF			5052	DC	XL16' 83FFFFFFFFFFFFFFFF 83FFFFFFFFFFFFFFFF'	result t
00005964	83FFFFFF FFFFFFFF						
				5053			
				5054	VRI_B	VGM 7, 0, 3	
00005970				5055+	DS	0FD	
00005970		00005970		5056+	USING	*, R5	base for test data and test routine
00005970	000059B8			5057+T167	DC	A(X167)	address of test routine
00005974	00A7			5058+	DC	H' 167'	test number
00005976	00			5059+	DC	X' 00'	
00005977	03			5060+	DC	HL1' 3'	M4 field
00005978	07			5061+	DC	HL1' 7'	i2 used
00005979	00			5062+	DC	HL1' 0'	i3 used
0000597A	E5C7D440 40404040			5063+	DC	CL8' VGM	instruction name
00005984	000059DC			5064+	DC	A(RE167+16)	address of v2 source
00005988	000059EC			5065+	DC	A(RE167+32)	address of v3 source
0000598C	00000010			5066+	DC	A(16)	result length
00005990	000059CC			5067+REA167	DC	A(RE167)	result address
00005998	00000000 00000000			5068+	DS	FD	gap
000059A0	00000000 00000000			5069+V10167	DS	XL16	V1 output
000059A8	00000000 00000000						
000059B0	00000000 00000000			5070+	DS	FD	gap
				5071+*			
000059B8				5072+X167	DS	0F	
000059B8	E760 8EAC 0806		000010AC	5073+	VL	V22, V1FUDGE	
000059BE	E760 0700 3846			5074+	VGM	V22, 7, 0, 3	test instruction (dest is a source)
000059C4	E760 5030 080E		000059A0	5075+	VST	V22, V10167	save v1 output
000059CA	07FB			5076+	BR	R11	return
000059CC				5077+RE167	DC	0F	xl16 expected result
000059CC				5078+	DROP	R5	
000059CC	81FFFFFF FFFFFFFF			5079	DC	XL16' 81FFFFFFFFFFFFFFFF 81FFFFFFFFFFFFFFFF'	result t
000059D4	81FFFFFF FFFFFFFF						
				5080			
				5081	VRI_B	VGM 8, 0, 3	
000059E0				5082+	DS	0FD	
000059E0		000059E0		5083+	USING	*, R5	base for test data and test routine
000059E0	00005A28			5084+T168	DC	A(X168)	address of test routine
000059E4	00A8			5085+	DC	H' 168'	test number
000059E6	00			5086+	DC	X' 00'	
000059E7	03			5087+	DC	HL1' 3'	M4 field
000059E8	08			5088+	DC	HL1' 8'	i2 used
000059E9	00			5089+	DC	HL1' 0'	i3 used
000059EA	E5C7D440 40404040			5090+	DC	CL8' VGM	instruction name
000059F4	00005A4C			5091+	DC	A(RE168+16)	address of v2 source
000059F8	00005A5C			5092+	DC	A(RE168+32)	address of v3 source
000059FC	00000010			5093+	DC	A(16)	result length
00005A00	00005A3C			5094+REA168	DC	A(RE168)	result address
00005A08	00000000 00000000			5095+	DS	FD	gap
00005A10	00000000 00000000			5096+V10168	DS	XL16	V1 output
00005A18	00000000 00000000						
00005A20	00000000 00000000			5097+	DS	FD	gap
				5098+*			
00005A28				5099+X168	DS	0F	
00005A28	E760 8EAC 0806		000010AC	5100+	VL	V22, V1FUDGE	
00005A2E	E760 0800 3846			5101+	VGM	V22, 8, 0, 3	test instruction (dest is a source)

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00005A34	E760 5030 080E		00005A10	5102+	VST	V22, V10168	save v1 output
00005A3A	07FB			5103+	BR	R11	return
00005A3C				5104+RE168	DC	0F	xl16 expected result
00005A3C				5105+	DROP	R5	
00005A3C	80FFFFFF FFFFFFFF			5106	DC	XL16' 80FFFFFFFFFFFFFFFF 80FFFFFFFFFFFFFFFF'	result t
00005A44	80FFFFFF FFFFFFFF						
				5107			
				5108	VRI_B	VGM 9, 0, 3	
00005A50				5109+	DS	0FD	
00005A50		00005A50		5110+	USING	*, R5	base for test data and test routine
00005A50	00005A98			5111+T169	DC	A(X169)	address of test routine
00005A54	00A9			5112+	DC	H' 169'	test number
00005A56	00			5113+	DC	X' 00'	
00005A57	03			5114+	DC	HL1' 3'	M4 field
00005A58	09			5115+	DC	HL1' 9'	i2 used
00005A59	00			5116+	DC	HL1' 0'	i3 used
00005A5A	E5C7D440 40404040			5117+	DC	CL8' VGM	instruction name
00005A64	00005ABC			5118+	DC	A(RE169+16)	address of v2 source
00005A68	00005ACC			5119+	DC	A(RE169+32)	address of v3 source
00005A6C	00000010			5120+	DC	A(16)	result length
00005A70	00005AAC			5121+REA169	DC	A(RE169)	result address
00005A78	00000000 00000000			5122+	DS	FD	gap
00005A80	00000000 00000000			5123+V10169	DS	XL16	V1 output
00005A88	00000000 00000000						
00005A90	00000000 00000000			5124+	DS	FD	gap
				5125+*			
00005A98				5126+X169	DS	0F	
00005A98	E760 8EAC 0806		000010AC	5127+	VL	V22, V1FUDGE	
00005A9E	E760 0900 3846			5128+	VGM	V22, 9, 0, 3	test instruction (dest is a source)
00005AA4	E760 5030 080E		00005A80	5129+	VST	V22, V10169	save v1 output
00005AAA	07FB			5130+	BR	R11	return
00005AAC				5131+RE169	DC	0F	xl16 expected result
00005AAC				5132+	DROP	R5	
00005AAC	807FFFFFF FFFFFFFF			5133	DC	XL16' 807FFFFFFFFFFFFFFFFF 807FFFFFFFFFFFFFFFF'	result t
00005AB4	807FFFFFF FFFFFFFF						
				5134			
				5135	VRI_B	VGM 11, 0, 3	
00005AC0				5136+	DS	0FD	
00005AC0		00005AC0		5137+	USING	*, R5	base for test data and test routine
00005AC0	00005B08			5138+T170	DC	A(X170)	address of test routine
00005AC4	00AA			5139+	DC	H' 170'	test number
00005AC6	00			5140+	DC	X' 00'	
00005AC7	03			5141+	DC	HL1' 3'	M4 field
00005AC8	0B			5142+	DC	HL1' 11'	i2 used
00005AC9	00			5143+	DC	HL1' 0'	i3 used
00005ACA	E5C7D440 40404040			5144+	DC	CL8' VGM	instruction name
00005AD4	00005B2C			5145+	DC	A(RE170+16)	address of v2 source
00005AD8	00005B3C			5146+	DC	A(RE170+32)	address of v3 source
00005ADC	00000010			5147+	DC	A(16)	result length
00005AE0	00005B1C			5148+REA170	DC	A(RE170)	result address
00005AE8	00000000 00000000			5149+	DS	FD	gap
00005AF0	00000000 00000000			5150+V10170	DS	XL16	V1 output
00005AF8	00000000 00000000						
00005B00	00000000 00000000			5151+	DS	FD	gap
				5152+*			
00005B08				5153+X170	DS	0F	



LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00005B08	E760 8EAC 0806		000010AC	5154+	VL	V22, V1FUDGE	
00005B0E	E760 0B00 3846			5155+	VGM	V22, 11, 0, 3	test instruction (dest is a source)
00005B14	E760 5030 080E		00005AF0	5156+	VST	V22, V10170	save v1 output
00005B1A	07FB			5157+	BR	R11	return
00005B1C				5158+RE170	DC	0F	xl16 expected result
00005B1C				5159+	DROP	R5	
00005B1C	801FFFFFF FFFFFFFF			5160	DC	XL16' 801FFFFFFFFFFFFFFF 801FFFFFFFFFFFFFFF'	result
00005B24	801FFFFFF FFFFFFFF						
				5161			
				5162	VRI_B	VGM, 13, 0, 3	
00005B30				5163+	DS	0FD	
00005B30		00005B30		5164+	USING	*, R5	base for test data and test routine
00005B30	00005B78			5165+T171	DC	A(X171)	address of test routine
00005B34	00AB			5166+	DC	H' 171'	test number
00005B36	00			5167+	DC	X' 00'	
00005B37	03			5168+	DC	HL1' 3'	M4 field
00005B38	0D			5169+	DC	HL1' 13'	i2 used
00005B39	00			5170+	DC	HL1' 0'	i3 used
00005B3A	E5C7D440 40404040			5171+	DC	CL8' VGM	instruction name
00005B44	00005B9C			5172+	DC	A(RE171+16)	address of v2 source
00005B48	00005BAC			5173+	DC	A(RE171+32)	address of v3 source
00005B4C	00000010			5174+	DC	A(16)	result length
00005B50	00005B8C			5175+REA171	DC	A(RE171)	result address
00005B58	00000000 00000000			5176+	DS	FD	gap
00005B60	00000000 00000000			5177+V10171	DS	XL16	V1 output
00005B68	00000000 00000000						
00005B70	00000000 00000000			5178+	DS	FD	gap
				5179+*			
00005B78				5180+X171	DS	0F	
00005B78	E760 8EAC 0806		000010AC	5181+	VL	V22, V1FUDGE	
00005B7E	E760 0D00 3846			5182+	VGM	V22, 13, 0, 3	test instruction (dest is a source)
00005B84	E760 5030 080E		00005B60	5183+	VST	V22, V10171	save v1 output
00005B8A	07FB			5184+	BR	R11	return
00005B8C				5185+RE171	DC	0F	xl16 expected result
00005B8C				5186+	DROP	R5	
00005B8C	8007FFFF FFFFFFFF			5187	DC	XL16' 8007FFFFFFFFFFFFFFF 8007FFFFFFFFFFFFFFF'	result
00005B94	8007FFFF FFFFFFFF						
				5188			
				5189	VRI_B	VGM, 15, 0, 3	
00005BA0				5190+	DS	0FD	
00005BA0		00005BA0		5191+	USING	*, R5	base for test data and test routine
00005BA0	00005BE8			5192+T172	DC	A(X172)	address of test routine
00005BA4	00AC			5193+	DC	H' 172'	test number
00005BA6	00			5194+	DC	X' 00'	
00005BA7	03			5195+	DC	HL1' 3'	M4 field
00005BA8	0F			5196+	DC	HL1' 15'	i2 used
00005BA9	00			5197+	DC	HL1' 0'	i3 used
00005BAA	E5C7D440 40404040			5198+	DC	CL8' VGM	instruction name
00005BB4	00005C0C			5199+	DC	A(RE172+16)	address of v2 source
00005BB8	00005C1C			5200+	DC	A(RE172+32)	address of v3 source
00005BBC	00000010			5201+	DC	A(16)	result length
00005BC0	00005BFC			5202+REA172	DC	A(RE172)	result address
00005BC8	00000000 00000000			5203+	DS	FD	gap
00005BD0	00000000 00000000			5204+V10172	DS	XL16	V1 output
00005BD8	00000000 00000000						
00005BE0	00000000 00000000			5205+	DS	FD	gap



LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00005BE8				5206+*			
00005BE8	E760 8EAC 0806		000010AC	5207+X172	DS	0F	
00005BEE	E760 0F00 3846			5208+	VL	V22, V1FUDGE	
00005BF4	E760 5030 080E		00005BD0	5209+	VGM	V22, 15, 0, 3	test instruction (dest is a source)
00005BFA	07FB			5210+	VST	V22, V10172	save v1 output
00005BFC				5211+	BR	R11	return
00005BFC				5212+RE172	DC	0F	xl16 expected result
00005BFC	8001FFFF FFFFFFFF			5213+	DROP	R5	
00005C04	8001FFFF FFFFFFFF			5214	DC	XL16' 8001FFFFFFFFFFFFFFF 8001FFFFFFFFFFFFFFF'	result t
				5215			
00005C10				5216	VRI_B	VGM, 16, 0, 3	
00005C10		00005C10		5217+	DS	0FD	
00005C10	00005C58			5218+	USING	*, R5	base for test data and test routine
00005C14	00AD			5219+T173	DC	A(X173)	address of test routine
00005C16	00			5220+	DC	H' 173'	test number
00005C17	03			5221+	DC	X' 00'	
00005C18	10			5222+	DC	HL1' 3'	M4 field
00005C19	00			5223+	DC	HL1' 16'	i2 used
00005C1A	E5C7D440 40404040			5224+	DC	HL1' 0'	i3 used
00005C24	00005C7C			5225+	DC	CL8' VGM	instruction name
00005C28	00005C8C			5226+	DC	A(RE173+16)	address of v2 source
00005C2C	00000010			5227+	DC	A(RE173+32)	address of v3 source
00005C30	00005C6C			5228+	DC	A(16)	result length
00005C38	00000000 00000000			5229+REA173	DC	A(RE173)	result address
00005C40	00000000 00000000			5230+	DS	FD	gap
00005C48	00000000 00000000			5231+V10173	DS	XL16	V1 output
00005C50	00000000 00000000			5232+	DS	FD	gap
				5233+*			
00005C58				5234+X173	DS	0F	
00005C58	E760 8EAC 0806		000010AC	5235+	VL	V22, V1FUDGE	
00005C5E	E760 1000 3846			5236+	VGM	V22, 16, 0, 3	test instruction (dest is a source)
00005C64	E760 5030 080E		00005C40	5237+	VST	V22, V10173	save v1 output
00005C6A	07FB			5238+	BR	R11	return
00005C6C				5239+RE173	DC	0F	xl16 expected result
00005C6C				5240+	DROP	R5	
00005C6C	8000FFFF FFFFFFFF			5241	DC	XL16' 8000FFFFFFFFFFFFFFF 8000FFFFFFFFFFFFFFF'	result t
00005C74	8000FFFF FFFFFFFF						
				5242			
00005C80				5243	VRI_B	VGM, 17, 0, 3	
00005C80		00005C80		5244+	DS	0FD	
00005C80	00005CC8			5245+	USING	*, R5	base for test data and test routine
00005C84	00AE			5246+T174	DC	A(X174)	address of test routine
00005C86	00			5247+	DC	H' 174'	test number
00005C87	03			5248+	DC	X' 00'	
00005C88	11			5249+	DC	HL1' 3'	M4 field
00005C89	00			5250+	DC	HL1' 17'	i2 used
00005C8A	E5C7D440 40404040			5251+	DC	HL1' 0'	i3 used
00005C94	00005CEC			5252+	DC	CL8' VGM	instruction name
00005C98	00005CFC			5253+	DC	A(RE174+16)	address of v2 source
00005C9C	00000010			5254+	DC	A(RE174+32)	address of v3 source
00005CA0	00005CDC			5255+	DC	A(16)	result length
00005CA8	00000000 00000000			5256+REA174	DC	A(RE174)	result address
00005CB0	00000000 00000000			5257+	DS	FD	gap
				5258+V10174	DS	XL16	V1 output

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00005CB8	00000000 00000000						
00005CC0	00000000 00000000			5259+	DS	FD	gap
				5260+*			
00005CC8				5261+X174	DS	OF	
00005CC8	E760 8EAC 0806		000010AC	5262+	VL	V22, V1FUDGE	
00005CCE	E760 1100 3846			5263+	VGM	V22, 17, 0, 3	test instruction (dest is a source)
00005CD4	E760 5030 080E		00005CB0	5264+	VST	V22, V10174	save v1 output
00005CDA	07FB			5265+	BR	R11	return
00005CDC				5266+RE174	DC	OF	xl16 expected result
00005CDC				5267+	DROP	R5	
00005CDC	80007FFF FFFFFFFF			5268	DC	XL16' 80007FFFFFFFFFFFFFFF 80007FFFFFFFFFFFFFFF'	result t
00005CE4	80007FFF FFFFFFFF						
				5269			
				5270	VRI_B	VGM, 25, 0, 3	
00005CF0				5271+	DS	OFD	
00005CF0		00005CF0		5272+	USING	*, R5	base for test data and test routine
00005CF0	00005D38			5273+T175	DC	A(X175)	address of test routine
00005CF4	00AF			5274+	DC	H' 175'	test number
00005CF6	00			5275+	DC	X' 00'	
00005CF7	03			5276+	DC	HL1' 3'	M4 field
00005CF8	19			5277+	DC	HL1' 25'	i2 used
00005CF9	00			5278+	DC	HL1' 0'	i3 used
00005CFA	E5C7D440 40404040			5279+	DC	CL8' VGM	instruction name
00005D04	00005D5C			5280+	DC	A(RE175+16)	address of v2 source
00005D08	00005D6C			5281+	DC	A(RE175+32)	address of v3 source
00005D0C	00000010			5282+	DC	A(16)	result length
00005D10	00005D4C			5283+REA175	DC	A(RE175)	result address
00005D18	00000000 00000000			5284+	DS	FD	gap
00005D20	00000000 00000000			5285+V10175	DS	XL16	V1 output
00005D28	00000000 00000000						
00005D30	00000000 00000000			5286+	DS	FD	gap
				5287+*			
00005D38				5288+X175	DS	OF	
00005D38	E760 8EAC 0806		000010AC	5289+	VL	V22, V1FUDGE	
00005D3E	E760 1900 3846			5290+	VGM	V22, 25, 0, 3	test instruction (dest is a source)
00005D44	E760 5030 080E		00005D20	5291+	VST	V22, V10175	save v1 output
00005D4A	07FB			5292+	BR	R11	return
00005D4C				5293+RE175	DC	OF	xl16 expected result
00005D4C				5294+	DROP	R5	
00005D4C	8000007F FFFFFFFF			5295	DC	XL16' 8000007FFFFFFFFFFFFFFF 8000007FFFFFFFFFFFFFFF'	result t
00005D54	8000007F FFFFFFFF						
				5296			
				5297	VRI_B	VGM, 30, 0, 3	
00005D60				5298+	DS	OFD	
00005D60		00005D60		5299+	USING	*, R5	base for test data and test routine
00005D60	00005DA8			5300+T176	DC	A(X176)	address of test routine
00005D64	00B0			5301+	DC	H' 176'	test number
00005D66	00			5302+	DC	X' 00'	
00005D67	03			5303+	DC	HL1' 3'	M4 field
00005D68	1E			5304+	DC	HL1' 30'	i2 used
00005D69	00			5305+	DC	HL1' 0'	i3 used
00005D6A	E5C7D440 40404040			5306+	DC	CL8' VGM	instruction name
00005D74	00005DCC			5307+	DC	A(RE176+16)	address of v2 source
00005D78	00005DDC			5308+	DC	A(RE176+32)	address of v3 source
00005D7C	00000010			5309+	DC	A(16)	result length
00005D80	00005DBC			5310+REA176	DC	A(RE176)	result address

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00005D88	00000000 00000000			5311+	DS	FD	gap
00005D90	00000000 00000000			5312+V10176	DS	XL16	V1 output
00005D98	00000000 00000000						
00005DA0	00000000 00000000			5313+	DS	FD	gap
				5314+*			
00005DA8				5315+X176	DS	OF	
00005DA8	E760 8EAC 0806		000010AC	5316+	VL	V22, V1FUDGE	
00005DAE	E760 1E00 3846			5317+	VGM	V22, 30, 0, 3	test instruction (dest is a source)
00005DB4	E760 5030 080E		00005D90	5318+	VST	V22, V10176	save v1 output
00005DBA	07FB			5319+	BR	R11	return
00005DBC				5320+RE176	DC	OF	xl16 expected result
00005DBC				5321+	DROP	R5	
00005DBC	80000003 FFFFFFFF			5322	DC	XL16' 80000003FFFFFFFF 80000003FFFFFFFF'	result
00005DC4	80000003 FFFFFFFF						
				5323			
				5324	VRI_B	VGM, 31, 0, 3	
00005DD0				5325+	DS	OFD	
00005DD0		00005DD0		5326+	USING	*, R5	base for test data and test routine
00005DD0	00005E18			5327+T177	DC	A(X177)	address of test routine
00005DD4	00B1			5328+	DC	H' 177'	test number
00005DD6	00			5329+	DC	X' 00'	
00005DD7	03			5330+	DC	HL1' 3'	M4 field
00005DD8	1F			5331+	DC	HL1' 31'	i2 used
00005DD9	00			5332+	DC	HL1' 0'	i3 used
00005DDA	E5C7D440 40404040			5333+	DC	CL8' VGM	instruction name
00005DE4	00005E3C			5334+	DC	A(RE177+16)	address of v2 source
00005DE8	00005E4C			5335+	DC	A(RE177+32)	address of v3 source
00005DEC	00000010			5336+	DC	A(16)	result length
00005DF0	00005E2C			5337+REA177	DC	A(RE177)	result address
00005DF8	00000000 00000000			5338+	DS	FD	gap
00005E00	00000000 00000000			5339+V10177	DS	XL16	V1 output
00005E08	00000000 00000000						
00005E10	00000000 00000000			5340+	DS	FD	gap
				5341+*			
00005E18				5342+X177	DS	OF	
00005E18	E760 8EAC 0806		000010AC	5343+	VL	V22, V1FUDGE	
00005E1E	E760 1F00 3846			5344+	VGM	V22, 31, 0, 3	test instruction (dest is a source)
00005E24	E760 5030 080E		00005E00	5345+	VST	V22, V10177	save v1 output
00005E2A	07FB			5346+	BR	R11	return
00005E2C				5347+RE177	DC	OF	xl16 expected result
00005E2C				5348+	DROP	R5	
00005E2C	80000001 FFFFFFFF			5349	DC	XL16' 80000001FFFFFFFF 80000001FFFFFFFF'	result
00005E34	80000001 FFFFFFFF						
				5350			
				5351	VRI_B	VGM, 33, 0, 3	
00005E40				5352+	DS	OFD	
00005E40		00005E40		5353+	USING	*, R5	base for test data and test routine
00005E40	00005E88			5354+T178	DC	A(X178)	address of test routine
00005E44	00B2			5355+	DC	H' 178'	test number
00005E46	00			5356+	DC	X' 00'	
00005E47	03			5357+	DC	HL1' 3'	M4 field
00005E48	21			5358+	DC	HL1' 33'	i2 used
00005E49	00			5359+	DC	HL1' 0'	i3 used
00005E4A	E5C7D440 40404040			5360+	DC	CL8' VGM	instruction name
00005E54	00005EAC			5361+	DC	A(RE178+16)	address of v2 source
00005E58	00005EBC			5362+	DC	A(RE178+32)	address of v3 source

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00005E5C	00000010			5363+	DC	A(16)	result length
00005E60	00005E9C			5364+REA178	DC	A(RE178)	result address
00005E68	00000000 00000000			5365+	DS	FD	gap
00005E70	00000000 00000000			5366+V10178	DS	XL16	V1 output
00005E78	00000000 00000000						
00005E80	00000000 00000000			5367+	DS	FD	gap
				5368+*			
00005E88				5369+X178	DS	0F	
00005E88	E760 8EAC 0806		000010AC	5370+	VL	V22, V1FUDGE	
00005E8E	E760 2100 3846			5371+	VGM	V22, 33, 0, 3	test instruction (dest is a source)
00005E94	E760 5030 080E		00005E70	5372+	VST	V22, V10178	save v1 output
00005E9A	07FB			5373+	BR	R11	return
00005E9C				5374+RE178	DC	0F	xl16 expected result
00005E9C				5375+	DROP	R5	
00005E9C	80000000 7FFFFFFF			5376	DC	XL16' 8000000007FFFFFFF 8000000007FFFFFFF'	result
00005EA4	80000000 7FFFFFFF						
				5377			
00005EB0				5378	VRI_B	VGM 55, 0, 3	
00005EB0		00005EB0		5379+	DS	0FD	
00005EB0	00005EF8			5380+	USING	*, R5	base for test data and test routine
00005EB4	00B3			5381+T179	DC	A(X179)	address of test routine
00005EB6	00			5382+	DC	H' 179'	test number
00005EB7	03			5383+	DC	X' 00'	
00005EB8	37			5384+	DC	HL1' 3'	M4 field
00005EB9	00			5385+	DC	HL1' 55'	i2 used
00005EBA	E5C7D440 40404040			5386+	DC	HL1' 0'	i3 used
00005EC4	00005F1C			5387+	DC	CL8' VGM	instruction name
00005EC8	00005F2C			5388+	DC	A(RE179+16)	address of v2 source
00005ECC	00000010			5389+	DC	A(RE179+32)	address of v3 source
00005ED0	00005F0C			5390+	DC	A(16)	result length
00005ED8	00000000 00000000			5391+REA179	DC	A(RE179)	result address
00005EE0	00000000 00000000			5392+	DS	FD	gap
00005EE8	00000000 00000000			5393+V10179	DS	XL16	V1 output
00005EF0	00000000 00000000						
				5394+	DS	FD	gap
				5395+*			
00005EF8				5396+X179	DS	0F	
00005EF8	E760 8EAC 0806		000010AC	5397+	VL	V22, V1FUDGE	
00005EFE	E760 3700 3846			5398+	VGM	V22, 55, 0, 3	test instruction (dest is a source)
00005F04	E760 5030 080E		00005EE0	5399+	VST	V22, V10179	save v1 output
00005F0A	07FB			5400+	BR	R11	return
00005F0C				5401+RE179	DC	0F	xl16 expected result
00005F0C				5402+	DROP	R5	
00005F0C	80000000 000001FF			5403	DC	XL16' 8000000000000001FF 8000000000000001FF'	result
00005F14	80000000 000001FF						
				5404			
00005F20				5405	VRI_B	VGM 62, 0, 3	
00005F20		00005F20		5406+	DS	0FD	
00005F20	00005F68			5407+	USING	*, R5	base for test data and test routine
00005F24	00B4			5408+T180	DC	A(X180)	address of test routine
00005F26	00			5409+	DC	H' 180'	test number
00005F27	03			5410+	DC	X' 00'	
00005F28	3E			5411+	DC	HL1' 3'	M4 field
00005F29	00			5412+	DC	HL1' 62'	i2 used
00005F2A	E5C7D440 40404040			5413+	DC	HL1' 0'	i3 used
				5414+	DC	CL8' VGM	instruction name





LOC	OBJECT CODE	ADDR1	ADDR2	STMT	
				5433 *Doubleword: I2>I3; I3=1	
				5434 VRI_B VGM 2, 1, 3	
00005F90				5435+ DS OFD	
00005F90		00005F90		5436+ USING *, R5	base for test data and test routine
00005F90	00005FD8			5437+T181 DC A(X181)	address of test routine
00005F94	00B5			5438+ DC H' 181'	test number
00005F96	00			5439+ DC X' 00'	
00005F97	03			5440+ DC HL1' 3'	M4 field
00005F98	02			5441+ DC HL1' 2'	i2 used
00005F99	01			5442+ DC HL1' 1'	i3 used
00005F9A	E5C7D440 40404040			5443+ DC CL8' VGM	instruction name
00005FA4	00005FFC			5444+ DC A(RE181+16)	address of v2 source
00005FA8	0000600C			5445+ DC A(RE181+32)	address of v3 source
00005FAC	00000010			5446+ DC A(16)	result length
00005FB0	00005FEC			5447+REA181 DC A(RE181)	result address
00005FB8	00000000 00000000			5448+ DS FD	gap
00005FC0	00000000 00000000			5449+V10181 DS XL16	V1 output
00005FC8	00000000 00000000				
00005FD0	00000000 00000000			5450+ DS FD	gap
				5451+*	
00005FD8				5452+X181 DS OF	
00005FD8	E760 8EAC 0806		000010AC	5453+ VL V22, V1FUDGE	
00005FDE	E760 0201 3846			5454+ VGM V22, 2, 1, 3	test instruction (dest is a source)
00005FE4	E760 5030 080E		00005FC0	5455+ VST V22, V10181	save v1 output
00005FEA	07FB			5456+ BR R11	return
00005FEC				5457+RE181 DC OF	xl16 expected result
00005FEC				5458+ DROP R5	
00005FEC	FFFFFFFF FFFFFFFF			5459 DC XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF'	result t
00005FF4	FFFFFFFF FFFFFFFF				
				5460	
				5461 VRI_B VGM 4, 1, 3	
00006000				5462+ DS OFD	
00006000		00006000		5463+ USING *, R5	base for test data and test routine
00006000	00006048			5464+T182 DC A(X182)	address of test routine
00006004	00B6			5465+ DC H' 182'	test number
00006006	00			5466+ DC X' 00'	
00006007	03			5467+ DC HL1' 3'	M4 field
00006008	04			5468+ DC HL1' 4'	i2 used
00006009	01			5469+ DC HL1' 1'	i3 used
0000600A	E5C7D440 40404040			5470+ DC CL8' VGM	instruction name
00006014	0000606C			5471+ DC A(RE182+16)	address of v2 source
00006018	0000607C			5472+ DC A(RE182+32)	address of v3 source
0000601C	00000010			5473+ DC A(16)	result length
00006020	0000605C			5474+REA182 DC A(RE182)	result address
00006028	00000000 00000000			5475+ DS FD	gap
00006030	00000000 00000000			5476+V10182 DS XL16	V1 output
00006038	00000000 00000000				
00006040	00000000 00000000			5477+ DS FD	gap
				5478+*	
00006048				5479+X182 DS OF	
00006048	E760 8EAC 0806		000010AC	5480+ VL V22, V1FUDGE	
0000604E	E760 0401 3846			5481+ VGM V22, 4, 1, 3	test instruction (dest is a source)
00006054	E760 5030 080E		00006030	5482+ VST V22, V10182	save v1 output
0000605A	07FB			5483+ BR R11	return
0000605C				5484+RE182 DC OF	xl16 expected result
0000605C				5485+ DROP R5	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
0000605C	CFFFFFFFF FFFFFFFF			5486	DC	XL16' CFFFFFFFFFFFFFFFFF CFFFFFFFFFFFFFFFFF'	result t
00006064	CFFFFFFFF FFFFFFFF						
				5487			
				5488	VRI_B	VGM 6, 1, 3	
00006070				5489+	DS	OFD	
00006070		00006070		5490+	USING	*, R5	base for test data and test routine
00006070	000060B8			5491+T183	DC	A(X183)	address of test routine
00006074	00B7			5492+	DC	H' 183'	test number
00006076	00			5493+	DC	X' 00'	
00006077	03			5494+	DC	HL1' 3'	M4 field
00006078	06			5495+	DC	HL1' 6'	i2 used
00006079	01			5496+	DC	HL1' 1'	i3 used
0000607A	E5C7D440 40404040			5497+	DC	CL8' VGM	instruction name
00006084	000060DC			5498+	DC	A(RE183+16)	address of v2 source
00006088	000060EC			5499+	DC	A(RE183+32)	address of v3 source
0000608C	00000010			5500+	DC	A(16)	result length
00006090	000060CC			5501+REA183	DC	A(RE183)	result address
00006098	00000000 00000000			5502+	DS	FD	gap
000060A0	00000000 00000000			5503+V10183	DS	XL16	V1 output
000060A8	00000000 00000000						
000060B0	00000000 00000000			5504+	DS	FD	gap
				5505+*			
000060B8				5506+X183	DS	OF	
000060B8	E760 8EAC 0806		000010AC	5507+	VL	V22, V1FUDGE	
000060BE	E760 0601 3846			5508+	VGM	V22, 6, 1, 3	test instruction (dest is a source)
000060C4	E760 5030 080E		000060A0	5509+	VST	V22, V10183	save v1 output
000060CA	07FB			5510+	BR	R11	return
000060CC				5511+RE183	DC	OF	xl16 expected result
000060CC				5512+	DROP	R5	
000060CC	C3FFFFFFFF FFFFFFFF			5513	DC	XL16' C3FFFFFFFFFFFFFFFFF C3FFFFFFFFFFFFFFFFF'	result t
000060D4	C3FFFFFFFF FFFFFFFF						
				5514			
				5515	VRI_B	VGM 7, 1, 3	
000060E0				5516+	DS	OFD	
000060E0		000060E0		5517+	USING	*, R5	base for test data and test routine
000060E0	00006128			5518+T184	DC	A(X184)	address of test routine
000060E4	00B8			5519+	DC	H' 184'	test number
000060E6	00			5520+	DC	X' 00'	
000060E7	03			5521+	DC	HL1' 3'	M4 field
000060E8	07			5522+	DC	HL1' 7'	i2 used
000060E9	01			5523+	DC	HL1' 1'	i3 used
000060EA	E5C7D440 40404040			5524+	DC	CL8' VGM	instruction name
000060F4	0000614C			5525+	DC	A(RE184+16)	address of v2 source
000060F8	0000615C			5526+	DC	A(RE184+32)	address of v3 source
000060FC	00000010			5527+	DC	A(16)	result length
00006100	0000613C			5528+REA184	DC	A(RE184)	result address
00006108	00000000 00000000			5529+	DS	FD	gap
00006110	00000000 00000000			5530+V10184	DS	XL16	V1 output
00006118	00000000 00000000						
00006120	00000000 00000000			5531+	DS	FD	gap
				5532+*			
00006128				5533+X184	DS	OF	
00006128	E760 8EAC 0806		000010AC	5534+	VL	V22, V1FUDGE	
0000612E	E760 0701 3846			5535+	VGM	V22, 7, 1, 3	test instruction (dest is a source)
00006134	E760 5030 080E		00006110	5536+	VST	V22, V10184	save v1 output
0000613A	07FB			5537+	BR	R11	return

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
0000613C				5538+RE184	DC	0F	xl16 expected result
0000613C				5539+	DROP	R5	
0000613C	C1FFFFFF FFFFFFFF			5540	DC	XL16' C1FFFFFFFFFFFFFFFF C1FFFFFFFFFFFFFFFF'	result t
00006144	C1FFFFFF FFFFFFFF						
				5541			
00006150				5542	VRI_B	VGM 8, 1, 3	
00006150		00006150		5543+	DS	0FD	
00006150	00006198			5544+	USING	*, R5	base for test data and test routine
00006154	00B9			5545+T185	DC	A(X185)	address of test routine
00006156	00			5546+	DC	H' 185'	test number
00006157	03			5547+	DC	X' 00'	
00006158	08			5548+	DC	HL1' 3'	M4 field
00006159	01			5549+	DC	HL1' 8'	i2 used
0000615A	E5C7D440 40404040			5550+	DC	HL1' 1'	i3 used
00006164	000061BC			5551+	DC	CL8' VGM	instruction name
00006168	000061CC			5552+	DC	A(RE185+16)	address of v2 source
0000616C	00000010			5553+	DC	A(RE185+32)	address of v3 source
00006170	000061AC			5554+	DC	A(16)	result length
00006178	00000000 00000000			5555+REA185	DC	A(RE185)	result address
00006180	00000000 00000000			5556+	DS	FD	gap
00006188	00000000 00000000			5557+V10185	DS	XL16	V1 output
00006190	00000000 00000000			5558+	DS	FD	gap
				5559+*			
00006198				5560+X185	DS	0F	
00006198	E760 8EAC 0806		000010AC	5561+	VL	V22, V1FUDGE	
0000619E	E760 0801 3846			5562+	VGM	V22, 8, 1, 3	test instruction (dest is a source)
000061A4	E760 5030 080E		00006180	5563+	VST	V22, V10185	save v1 output
000061AA	07FB			5564+	BR	R11	return
000061AC				5565+RE185	DC	0F	xl16 expected result
000061AC				5566+	DROP	R5	
000061AC	C0FFFFFF FFFFFFFF			5567	DC	XL16' C0FFFFFFFFFFFFFFFF C0FFFFFFFFFFFFFFFF'	result t
000061B4	C0FFFFFF FFFFFFFF						
				5568			
000061C0				5569	VRI_B	VGM 9, 1, 3	
000061C0		000061C0		5570+	DS	0FD	
000061C0	00006208			5571+	USING	*, R5	base for test data and test routine
000061C4	00BA			5572+T186	DC	A(X186)	address of test routine
000061C6	00			5573+	DC	H' 186'	test number
000061C7	00			5574+	DC	X' 00'	
000061C8	03			5575+	DC	HL1' 3'	M4 field
000061C9	09			5576+	DC	HL1' 9'	i2 used
000061CA	01			5577+	DC	HL1' 1'	i3 used
000061CA	E5C7D440 40404040			5578+	DC	CL8' VGM	instruction name
000061D4	0000622C			5579+	DC	A(RE186+16)	address of v2 source
000061D8	0000623C			5580+	DC	A(RE186+32)	address of v3 source
000061DC	00000010			5581+	DC	A(16)	result length
000061E0	0000621C			5582+REA186	DC	A(RE186)	result address
000061E8	00000000 00000000			5583+	DS	FD	gap
000061F0	00000000 00000000			5584+V10186	DS	XL16	V1 output
000061F8	00000000 00000000						
00006200	00000000 00000000			5585+	DS	FD	gap
				5586+*			
00006208				5587+X186	DS	0F	
00006208	E760 8EAC 0806		000010AC	5588+	VL	V22, V1FUDGE	
0000620E	E760 0901 3846			5589+	VGM	V22, 9, 1, 3	test instruction (dest is a source)

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00006214	E760 5030 080E		000061F0	5590+	VST	V22, V10186	save v1 output
0000621A	07FB			5591+	BR	R11	return
0000621C				5592+RE186	DC	0F	xl16 expected result
0000621C				5593+	DROP	R5	
0000621C	C07FFFFFFF FFFFFFFF			5594	DC	XL16' C07FFFFFFFFFFFFFFFF C07FFFFFFFFFFFFFFFF'	result t
00006224	C07FFFFFFF FFFFFFFF						
				5595			
				5596	VRI_B	VGM, 11, 1, 3	
00006230				5597+	DS	0FD	
00006230		00006230		5598+	USING	*, R5	base for test data and test routine
00006230	00006278			5599+T187	DC	A(X187)	address of test routine
00006234	00BB			5600+	DC	H' 187'	test number
00006236	00			5601+	DC	X' 00'	
00006237	03			5602+	DC	HL1' 3'	M4 field
00006238	0B			5603+	DC	HL1' 11'	i2 used
00006239	01			5604+	DC	HL1' 1'	i3 used
0000623A	E5C7D440 40404040			5605+	DC	CL8' VGM	instruction name
00006244	0000629C			5606+	DC	A(RE187+16)	address of v2 source
00006248	000062AC			5607+	DC	A(RE187+32)	address of v3 source
0000624C	00000010			5608+	DC	A(16)	result length
00006250	0000628C			5609+REA187	DC	A(RE187)	result address
00006258	00000000 00000000			5610+	DS	FD	gap
00006260	00000000 00000000			5611+V10187	DS	XL16	V1 output
00006268	00000000 00000000						
00006270	00000000 00000000			5612+	DS	FD	gap
				5613+*			
00006278				5614+X187	DS	0F	
00006278	E760 8EAC 0806		000010AC	5615+	VL	V22, V1FUDGE	
0000627E	E760 0B01 3846			5616+	VGM	V22, 11, 1, 3	test instruction (dest is a source)
00006284	E760 5030 080E		00006260	5617+	VST	V22, V10187	save v1 output
0000628A	07FB			5618+	BR	R11	return
0000628C				5619+RE187	DC	0F	xl16 expected result
0000628C				5620+	DROP	R5	
0000628C	C01FFFFFFF FFFFFFFF			5621	DC	XL16' C01FFFFFFFFFFFFFFFF C01FFFFFFFFFFFFFFFF'	result t
00006294	C01FFFFFFF FFFFFFFF						
				5622			
				5623	VRI_B	VGM, 13, 1, 3	
000062A0				5624+	DS	0FD	
000062A0		000062A0		5625+	USING	*, R5	base for test data and test routine
000062A0	000062E8			5626+T188	DC	A(X188)	address of test routine
000062A4	00BC			5627+	DC	H' 188'	test number
000062A6	00			5628+	DC	X' 00'	
000062A7	03			5629+	DC	HL1' 3'	M4 field
000062A8	0D			5630+	DC	HL1' 13'	i2 used
000062A9	01			5631+	DC	HL1' 1'	i3 used
000062AA	E5C7D440 40404040			5632+	DC	CL8' VGM	instruction name
000062B4	0000630C			5633+	DC	A(RE188+16)	address of v2 source
000062B8	0000631C			5634+	DC	A(RE188+32)	address of v3 source
000062BC	00000010			5635+	DC	A(16)	result length
000062C0	000062FC			5636+REA188	DC	A(RE188)	result address
000062C8	00000000 00000000			5637+	DS	FD	gap
000062D0	00000000 00000000			5638+V10188	DS	XL16	V1 output
000062D8	00000000 00000000						
000062E0	00000000 00000000			5639+	DS	FD	gap
				5640+*			
000062E8				5641+X188	DS	0F	



LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
000062E8	E760 8EAC 0806		000010AC	5642+	VL	V22, V1FUDGE	
000062EE	E760 0D01 3846			5643+	VGM	V22, 13, 1, 3	test instruction (dest is a source)
000062F4	E760 5030 080E		000062D0	5644+	VST	V22, V10188	save v1 output
000062FA	07FB			5645+	BR	R11	return
000062FC				5646+RE188	DC	0F	xl16 expected result
000062FC				5647+	DROP	R5	
000062FC	C007FFFF FFFFFFFF			5648	DC	XL16' C007FFFFFFFFFFFFFFFF C007FFFFFFFFFFFFFFFF'	result
00006304	C007FFFF FFFFFFFF						
				5649			
				5650	VRI_B	VGM, 15, 1, 3	
00006310				5651+	DS	0FD	
00006310		00006310		5652+	USING	*, R5	base for test data and test routine
00006310	00006358			5653+T189	DC	A(X189)	address of test routine
00006314	00BD			5654+	DC	H' 189'	test number
00006316	00			5655+	DC	X' 00'	
00006317	03			5656+	DC	HL1' 3'	M4 field
00006318	0F			5657+	DC	HL1' 15'	i2 used
00006319	01			5658+	DC	HL1' 1'	i3 used
0000631A	E5C7D440 40404040			5659+	DC	CL8' VGM	instruction name
00006324	0000637C			5660+	DC	A(RE189+16)	address of v2 source
00006328	0000638C			5661+	DC	A(RE189+32)	address of v3 source
0000632C	00000010			5662+	DC	A(16)	result length
00006330	0000636C			5663+REA189	DC	A(RE189)	result address
00006338	00000000 00000000			5664+	DS	FD	gap
00006340	00000000 00000000			5665+V10189	DS	XL16	V1 output
00006348	00000000 00000000						
00006350	00000000 00000000			5666+	DS	FD	gap
				5667+*			
00006358				5668+X189	DS	0F	
00006358	E760 8EAC 0806		000010AC	5669+	VL	V22, V1FUDGE	
0000635E	E760 0F01 3846			5670+	VGM	V22, 15, 1, 3	test instruction (dest is a source)
00006364	E760 5030 080E		00006340	5671+	VST	V22, V10189	save v1 output
0000636A	07FB			5672+	BR	R11	return
0000636C				5673+RE189	DC	0F	xl16 expected result
0000636C				5674+	DROP	R5	
0000636C	C001FFFF FFFFFFFF			5675	DC	XL16' C001FFFFFFFFFFFFFFFF C001FFFFFFFFFFFFFFFF'	result
00006374	C001FFFF FFFFFFFF						
				5676			
				5677	VRI_B	VGM, 16, 1, 3	
00006380				5678+	DS	0FD	
00006380		00006380		5679+	USING	*, R5	base for test data and test routine
00006380	000063C8			5680+T190	DC	A(X190)	address of test routine
00006384	00BE			5681+	DC	H' 190'	test number
00006386	00			5682+	DC	X' 00'	
00006387	03			5683+	DC	HL1' 3'	M4 field
00006388	10			5684+	DC	HL1' 16'	i2 used
00006389	01			5685+	DC	HL1' 1'	i3 used
0000638A	E5C7D440 40404040			5686+	DC	CL8' VGM	instruction name
00006394	000063EC			5687+	DC	A(RE190+16)	address of v2 source
00006398	000063FC			5688+	DC	A(RE190+32)	address of v3 source
0000639C	00000010			5689+	DC	A(16)	result length
000063A0	000063DC			5690+REA190	DC	A(RE190)	result address
000063A8	00000000 00000000			5691+	DS	FD	gap
000063B0	00000000 00000000			5692+V10190	DS	XL16	V1 output
000063B8	00000000 00000000						
000063C0	00000000 00000000			5693+	DS	FD	gap



LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
000063C8				5694+*			
000063C8	E760 8EAC 0806		000010AC	5695+X190	DS	0F	
000063CE	E760 1001 3846			5696+	VL	V22, V1FUDGE	
000063D4	E760 5030 080E		000063B0	5697+	VGM	V22, 16, 1, 3	test instruction (dest is a source)
000063DA	07FB			5698+	VST	V22, V10190	save v1 output
000063DC				5699+	BR	R11	return
000063DC				5700+RE190	DC	0F	xl16 expected result
000063DC	C000FFFF FFFFFFFF			5701+	DROP	R5	
000063E4	C000FFFF FFFFFFFF			5702	DC	XL16' C000FFFFFFFFFFFFFFFF C000FFFFFFFFFFFFFFFF'	result t
				5703			
000063F0				5704	VRI_B	VGM, 17, 1, 3	
000063F0		000063F0		5705+	DS	0FD	
000063F0	00006438			5706+	USING	*, R5	base for test data and test routine
000063F4	00BF			5707+T191	DC	A(X191)	address of test routine
000063F6	00			5708+	DC	H' 191'	test number
000063F7	03			5709+	DC	X' 00'	
000063F8	11			5710+	DC	HL1' 3'	M4 field
000063F9	01			5711+	DC	HL1' 17'	i2 used
000063FA	E5C7D440 40404040			5712+	DC	HL1' 1'	i3 used
00006404	0000645C			5713+	DC	CL8' VGM	instruction name
00006408	0000646C			5714+	DC	A(RE191+16)	address of v2 source
0000640C	00000010			5715+	DC	A(RE191+32)	address of v3 source
00006410	0000644C			5716+	DC	A(16)	result length
00006418	00000000 00000000			5717+REA191	DC	A(RE191)	result address
00006420	00000000 00000000			5718+	DS	FD	gap
00006428	00000000 00000000			5719+V10191	DS	XL16	V1 output
00006430	00000000 00000000			5720+	DS	FD	gap
				5721+*			
00006438				5722+X191	DS	0F	
00006438	E760 8EAC 0806		000010AC	5723+	VL	V22, V1FUDGE	
0000643E	E760 1101 3846			5724+	VGM	V22, 17, 1, 3	test instruction (dest is a source)
00006444	E760 5030 080E		00006420	5725+	VST	V22, V10191	save v1 output
0000644A	07FB			5726+	BR	R11	return
0000644C				5727+RE191	DC	0F	xl16 expected result
0000644C				5728+	DROP	R5	
0000644C	C0007FFF FFFFFFFF			5729	DC	XL16' C0007FFFFFFFFFFFFFFFF C0007FFFFFFFFFFFFFFFF'	result t
00006454	C0007FFF FFFFFFFF						
				5730			
00006460				5731	VRI_B	VGM, 25, 1, 3	
00006460		00006460		5732+	DS	0FD	
00006460	000064A8			5733+	USING	*, R5	base for test data and test routine
00006464	00C0			5734+T192	DC	A(X192)	address of test routine
00006466	00			5735+	DC	H' 192'	test number
00006467	03			5736+	DC	X' 00'	
00006468	19			5737+	DC	HL1' 3'	M4 field
00006469	01			5738+	DC	HL1' 25'	i2 used
0000646A	E5C7D440 40404040			5739+	DC	HL1' 1'	i3 used
00006474	000064CC			5740+	DC	CL8' VGM	instruction name
00006478	000064DC			5741+	DC	A(RE192+16)	address of v2 source
0000647C	00000010			5742+	DC	A(RE192+32)	address of v3 source
00006480	000064BC			5743+	DC	A(16)	result length
00006488	00000000 00000000			5744+REA192	DC	A(RE192)	result address
00006490	00000000 00000000			5745+	DS	FD	gap
				5746+V10192	DS	XL16	V1 output

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00006498	00000000 00000000						
000064A0	00000000 00000000			5747+	DS	FD	gap
				5748+*			
000064A8				5749+X192	DS	0F	
000064A8	E760 8EAC 0806		000010AC	5750+	VL	V22, V1FUDGE	
000064AE	E760 1901 3846			5751+	VGM	V22, 25, 1, 3	test instruction (dest is a source)
000064B4	E760 5030 080E		00006490	5752+	VST	V22, V10192	save v1 output
000064BA	07FB			5753+	BR	R11	return
000064BC				5754+RE192	DC	0F	xl16 expected result
000064BC				5755+	DROP	R5	
000064BC	C000007F FFFFFFFF			5756	DC	XL16' C000007FFFFFFFFF C000007FFFFFFFFF'	result t
000064C4	C000007F FFFFFFFF						
				5757			
				5758	VRI_B	VGM, 30, 1, 3	
000064D0				5759+	DS	0FD	
000064D0		000064D0		5760+	USING	*, R5	base for test data and test routine
000064D0	00006518			5761+T193	DC	A(X193)	address of test routine
000064D4	00C1			5762+	DC	H' 193'	test number
000064D6	00			5763+	DC	X' 00'	
000064D7	03			5764+	DC	HL1' 3'	M4 field
000064D8	1E			5765+	DC	HL1' 30'	i2 used
000064D9	01			5766+	DC	HL1' 1'	i3 used
000064DA	E5C7D440 40404040			5767+	DC	CL8' VGM	instruction name
000064E4	0000653C			5768+	DC	A(RE193+16)	address of v2 source
000064E8	0000654C			5769+	DC	A(RE193+32)	address of v3 source
000064EC	00000010			5770+	DC	A(16)	result length
000064F0	0000652C			5771+REA193	DC	A(RE193)	result address
000064F8	00000000 00000000			5772+	DS	FD	gap
00006500	00000000 00000000			5773+V10193	DS	XL16	V1 output
00006508	00000000 00000000						
00006510	00000000 00000000			5774+	DS	FD	gap
				5775+*			
00006518				5776+X193	DS	0F	
00006518	E760 8EAC 0806		000010AC	5777+	VL	V22, V1FUDGE	
0000651E	E760 1E01 3846			5778+	VGM	V22, 30, 1, 3	test instruction (dest is a source)
00006524	E760 5030 080E		00006500	5779+	VST	V22, V10193	save v1 output
0000652A	07FB			5780+	BR	R11	return
0000652C				5781+RE193	DC	0F	xl16 expected result
0000652C				5782+	DROP	R5	
0000652C	C0000003 FFFFFFFF			5783	DC	XL16' C0000003FFFFFFFFF C0000003FFFFFFFFF'	result t
00006534	C0000003 FFFFFFFF						
				5784			
				5785	VRI_B	VGM, 31, 1, 3	
00006540				5786+	DS	0FD	
00006540		00006540		5787+	USING	*, R5	base for test data and test routine
00006540	00006588			5788+T194	DC	A(X194)	address of test routine
00006544	00C2			5789+	DC	H' 194'	test number
00006546	00			5790+	DC	X' 00'	
00006547	03			5791+	DC	HL1' 3'	M4 field
00006548	1F			5792+	DC	HL1' 31'	i2 used
00006549	01			5793+	DC	HL1' 1'	i3 used
0000654A	E5C7D440 40404040			5794+	DC	CL8' VGM	instruction name
00006554	000065AC			5795+	DC	A(RE194+16)	address of v2 source
00006558	000065BC			5796+	DC	A(RE194+32)	address of v3 source
0000655C	00000010			5797+	DC	A(16)	result length
00006560	0000659C			5798+REA194	DC	A(RE194)	result address

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00006568	00000000 00000000			5799+	DS	FD	gap
00006570	00000000 00000000			5800+V10194	DS	XL16	V1 output
00006578	00000000 00000000						
00006580	00000000 00000000			5801+	DS	FD	gap
				5802+*			
00006588				5803+X194	DS	OF	
00006588	E760 8EAC 0806		000010AC	5804+	VL	V22, V1FUDGE	
0000658E	E760 1F01 3846			5805+	VGM	V22, 31, 1, 3	test instruction (dest is a source)
00006594	E760 5030 080E		00006570	5806+	VST	V22, V10194	save v1 output
0000659A	07FB			5807+	BR	R11	return
0000659C				5808+RE194	DC	OF	xl16 expected result
0000659C				5809+	DROP	R5	
0000659C	C0000001 FFFFFFFF			5810	DC	XL16' C0000001FFFFFFFF C0000001FFFFFFFF'	result
000065A4	C0000001 FFFFFFFF						
				5811			
				5812	VRI_B	VGM, 33, 1, 3	
000065B0				5813+	DS	OFD	
000065B0		000065B0		5814+	USING	*, R5	base for test data and test routine
000065B0	000065F8			5815+T195	DC	A(X195)	address of test routine
000065B4	00C3			5816+	DC	H' 195'	test number
000065B6	00			5817+	DC	X' 00'	
000065B7	03			5818+	DC	HL1' 3'	M4 field
000065B8	21			5819+	DC	HL1' 33'	i2 used
000065B9	01			5820+	DC	HL1' 1'	i3 used
000065BA	E5C7D440 40404040			5821+	DC	CL8' VGM	instruction name
000065C4	0000661C			5822+	DC	A(RE195+16)	address of v2 source
000065C8	0000662C			5823+	DC	A(RE195+32)	address of v3 source
000065CC	00000010			5824+	DC	A(16)	result length
000065D0	0000660C			5825+REA195	DC	A(RE195)	result address
000065D8	00000000 00000000			5826+	DS	FD	gap
000065E0	00000000 00000000			5827+V10195	DS	XL16	V1 output
000065E8	00000000 00000000						
000065F0	00000000 00000000			5828+	DS	FD	gap
				5829+*			
000065F8				5830+X195	DS	OF	
000065F8	E760 8EAC 0806		000010AC	5831+	VL	V22, V1FUDGE	
000065FE	E760 2101 3846			5832+	VGM	V22, 33, 1, 3	test instruction (dest is a source)
00006604	E760 5030 080E		000065E0	5833+	VST	V22, V10195	save v1 output
0000660A	07FB			5834+	BR	R11	return
0000660C				5835+RE195	DC	OF	xl16 expected result
0000660C				5836+	DROP	R5	
0000660C	C0000000 7FFFFFFF			5837	DC	XL16' C00000007FFFFFFF C00000007FFFFFFF'	result
00006614	C0000000 7FFFFFFF						
				5838			
				5839	VRI_B	VGM, 55, 1, 3	
00006620				5840+	DS	OFD	
00006620		00006620		5841+	USING	*, R5	base for test data and test routine
00006620	00006668			5842+T196	DC	A(X196)	address of test routine
00006624	00C4			5843+	DC	H' 196'	test number
00006626	00			5844+	DC	X' 00'	
00006627	03			5845+	DC	HL1' 3'	M4 field
00006628	37			5846+	DC	HL1' 55'	i2 used
00006629	01			5847+	DC	HL1' 1'	i3 used
0000662A	E5C7D440 40404040			5848+	DC	CL8' VGM	instruction name
00006634	0000668C			5849+	DC	A(RE196+16)	address of v2 source
00006638	0000669C			5850+	DC	A(RE196+32)	address of v3 source

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
0000663C	00000010			5851+	DC	A(16)	result length
00006640	0000667C			5852+REA196	DC	A(RE196)	result address
00006648	00000000 00000000			5853+	DS	FD	gap
00006650	00000000 00000000			5854+V10196	DS	XL16	V1 output
00006658	00000000 00000000						
00006660	00000000 00000000			5855+	DS	FD	gap
				5856+*			
00006668				5857+X196	DS	OF	
00006668	E760 8EAC 0806		000010AC	5858+	VL	V22, V1FUDGE	
0000666E	E760 3701 3846			5859+	VGM	V22, 55, 1, 3	test instruction (dest is a source)
00006674	E760 5030 080E		00006650	5860+	VST	V22, V10196	save v1 output
0000667A	07FB			5861+	BR	R11	return
0000667C				5862+RE196	DC	OF	xl16 expected result
0000667C				5863+	DROP	R5	
0000667C	C0000000 000001FF			5864	DC	XL16' C000000000000001FF C000000000000001FF'	result t
00006684	C0000000 000001FF						
				5865			
00006690				5866	VRI_B	VGM 62, 1, 3	
00006690		00006690		5867+	DS	OFD	
00006690	000066D8			5868+	USING	*, R5	base for test data and test routine
00006694	00C5			5869+T197	DC	A(X197)	address of test routine
00006696	00			5870+	DC	H' 197'	test number
00006696	00			5871+	DC	X' 00'	
00006697	03			5872+	DC	HL1' 3'	M4 field
00006698	3E			5873+	DC	HL1' 62'	i2 used
00006699	01			5874+	DC	HL1' 1'	i3 used
0000669A	E5C7D440 40404040			5875+	DC	CL8' VGM	instruction name
000066A4	000066FC			5876+	DC	A(RE197+16)	address of v2 source
000066A8	0000670C			5877+	DC	A(RE197+32)	address of v3 source
000066AC	00000010			5878+	DC	A(16)	result length
000066B0	000066EC			5879+REA197	DC	A(RE197)	result address
000066B8	00000000 00000000			5880+	DS	FD	gap
000066C0	00000000 00000000			5881+V10197	DS	XL16	V1 output
000066C8	00000000 00000000						
000066D0	00000000 00000000			5882+	DS	FD	gap
				5883+*			
000066D8				5884+X197	DS	OF	
000066D8	E760 8EAC 0806		000010AC	5885+	VL	V22, V1FUDGE	
000066DE	E760 3E01 3846			5886+	VGM	V22, 62, 1, 3	test instruction (dest is a source)
000066E4	E760 5030 080E		000066C0	5887+	VST	V22, V10197	save v1 output
000066EA	07FB			5888+	BR	R11	return
000066EC				5889+RE197	DC	OF	xl16 expected result
000066EC				5890+	DROP	R5	
000066EC	C0000000 00000003			5891	DC	XL16' C00000000000000003 C00000000000000003'	result t
000066F4	C0000000 00000003						
				5892			
				5893			
				5894			
000066FC	00000000			5895	DC	F' 0'	END OF TABLE
00006700	00000000			5896	DC	F' 0'	



LOC	OBJECT CODE	ADDR1	ADDR2	STMT
				5898 *
				5899 * table of pointers to individual load test
				5900 *
00006704				5901 E7TESTS DS OF
				5902 PTTABLE
00006704				5903+TTABLE DS OF
00006704	000010D0			5904+ DC A(T1)
00006708	00001140			5905+ DC A(T2)
0000670C	000011B0			5906+ DC A(T3)
00006710	00001220			5907+ DC A(T4)
00006714	00001290			5908+ DC A(T5)
00006718	00001300			5909+ DC A(T6)
0000671C	00001370			5910+ DC A(T7)
00006720	000013E0			5911+ DC A(T8)
00006724	00001450			5912+ DC A(T9)
00006728	000014C0			5913+ DC A(T10)
0000672C	00001530			5914+ DC A(T11)
00006730	000015A0			5915+ DC A(T12)
00006734	00001610			5916+ DC A(T13)
00006738	00001680			5917+ DC A(T14)
0000673C	000016F0			5918+ DC A(T15)
00006740	00001760			5919+ DC A(T16)
00006744	000017D0			5920+ DC A(T17)
00006748	00001840			5921+ DC A(T18)
0000674C	000018B0			5922+ DC A(T19)
00006750	00001920			5923+ DC A(T20)
00006754	00001990			5924+ DC A(T21)
00006758	00001A00			5925+ DC A(T22)
0000675C	00001A70			5926+ DC A(T23)
00006760	00001AE0			5927+ DC A(T24)
00006764	00001B50			5928+ DC A(T25)
00006768	00001BC0			5929+ DC A(T26)
0000676C	00001C30			5930+ DC A(T27)
00006770	00001CA0			5931+ DC A(T28)
00006774	00001D10			5932+ DC A(T29)
00006778	00001D80			5933+ DC A(T30)
0000677C	00001DF0			5934+ DC A(T31)
00006780	00001E60			5935+ DC A(T32)
00006784	00001ED0			5936+ DC A(T33)
00006788	00001F40			5937+ DC A(T34)
0000678C	00001FB0			5938+ DC A(T35)
00006790	00002020			5939+ DC A(T36)
00006794	00002090			5940+ DC A(T37)
00006798	00002100			5941+ DC A(T38)
0000679C	00002170			5942+ DC A(T39)
000067A0	000021E0			5943+ DC A(T40)
000067A4	00002250			5944+ DC A(T41)
000067A8	000022C0			5945+ DC A(T42)
000067AC	00002330			5946+ DC A(T43)
000067B0	000023A0			5947+ DC A(T44)
000067B4	00002410			5948+ DC A(T45)
000067B8	00002480			5949+ DC A(T46)
000067BC	000024F0			5950+ DC A(T47)
000067C0	00002560			5951+ DC A(T48)
000067C4	000025D0			5952+ DC A(T49)
000067C8	00002640			5953+ DC A(T50)



LOC	OBJECT CODE	ADDR1	ADDR2	STMT	
000067CC	000026B0			5954+	DC A(T51)
000067D0	00002720			5955+	DC A(T52)
000067D4	00002790			5956+	DC A(T53)
000067D8	00002800			5957+	DC A(T54)
000067DC	00002870			5958+	DC A(T55)
000067E0	000028E0			5959+	DC A(T56)
000067E4	00002950			5960+	DC A(T57)
000067E8	000029C0			5961+	DC A(T58)
000067EC	00002A30			5962+	DC A(T59)
000067F0	00002AA0			5963+	DC A(T60)
000067F4	00002B10			5964+	DC A(T61)
000067F8	00002B80			5965+	DC A(T62)
000067FC	00002BF0			5966+	DC A(T63)
00006800	00002C60			5967+	DC A(T64)
00006804	00002CD0			5968+	DC A(T65)
00006808	00002D40			5969+	DC A(T66)
0000680C	00002DB0			5970+	DC A(T67)
00006810	00002E20			5971+	DC A(T68)
00006814	00002E90			5972+	DC A(T69)
00006818	00002F00			5973+	DC A(T70)
0000681C	00002F70			5974+	DC A(T71)
00006820	00002FE0			5975+	DC A(T72)
00006824	00003050			5976+	DC A(T73)
00006828	000030C0			5977+	DC A(T74)
0000682C	00003130			5978+	DC A(T75)
00006830	000031A0			5979+	DC A(T76)
00006834	00003210			5980+	DC A(T77)
00006838	00003280			5981+	DC A(T78)
0000683C	000032F0			5982+	DC A(T79)
00006840	00003360			5983+	DC A(T80)
00006844	000033D0			5984+	DC A(T81)
00006848	00003440			5985+	DC A(T82)
0000684C	000034B0			5986+	DC A(T83)
00006850	00003520			5987+	DC A(T84)
00006854	00003590			5988+	DC A(T85)
00006858	00003600			5989+	DC A(T86)
0000685C	00003670			5990+	DC A(T87)
00006860	000036E0			5991+	DC A(T88)
00006864	00003750			5992+	DC A(T89)
00006868	000037C0			5993+	DC A(T90)
0000686C	00003830			5994+	DC A(T91)
00006870	000038A0			5995+	DC A(T92)
00006874	00003910			5996+	DC A(T93)
00006878	00003980			5997+	DC A(T94)
0000687C	000039F0			5998+	DC A(T95)
00006880	00003A60			5999+	DC A(T96)
00006884	00003AD0			6000+	DC A(T97)
00006888	00003B40			6001+	DC A(T98)
0000688C	00003BB0			6002+	DC A(T99)
00006890	00003C20			6003+	DC A(T100)
00006894	00003C90			6004+	DC A(T101)
00006898	00003D00			6005+	DC A(T102)
0000689C	00003D70			6006+	DC A(T103)
000068A0	00003DE0			6007+	DC A(T104)
000068A4	00003E50			6008+	DC A(T105)
000068A8	00003EC0			6009+	DC A(T106)

LOC	OBJECT CODE	ADDR1	ADDR2	STMT		
000068AC	00003F30			6010+	DC	A(T107)
000068B0	00003FA0			6011+	DC	A(T108)
000068B4	00004010			6012+	DC	A(T109)
000068B8	00004080			6013+	DC	A(T110)
000068BC	000040F0			6014+	DC	A(T111)
000068C0	00004160			6015+	DC	A(T112)
000068C4	000041D0			6016+	DC	A(T113)
000068C8	00004240			6017+	DC	A(T114)
000068CC	000042B0			6018+	DC	A(T115)
000068D0	00004320			6019+	DC	A(T116)
000068D4	00004390			6020+	DC	A(T117)
000068D8	00004400			6021+	DC	A(T118)
000068DC	00004470			6022+	DC	A(T119)
000068E0	000044E0			6023+	DC	A(T120)
000068E4	00004550			6024+	DC	A(T121)
000068E8	000045C0			6025+	DC	A(T122)
000068EC	00004630			6026+	DC	A(T123)
000068F0	000046A0			6027+	DC	A(T124)
000068F4	00004710			6028+	DC	A(T125)
000068F8	00004780			6029+	DC	A(T126)
000068FC	000047F0			6030+	DC	A(T127)
00006900	00004860			6031+	DC	A(T128)
00006904	000048D0			6032+	DC	A(T129)
00006908	00004940			6033+	DC	A(T130)
0000690C	000049B0			6034+	DC	A(T131)
00006910	00004A20			6035+	DC	A(T132)
00006914	00004A90			6036+	DC	A(T133)
00006918	00004B00			6037+	DC	A(T134)
0000691C	00004B70			6038+	DC	A(T135)
00006920	00004BE0			6039+	DC	A(T136)
00006924	00004C50			6040+	DC	A(T137)
00006928	00004CC0			6041+	DC	A(T138)
0000692C	00004D30			6042+	DC	A(T139)
00006930	00004DA0			6043+	DC	A(T140)
00006934	00004E10			6044+	DC	A(T141)
00006938	00004E80			6045+	DC	A(T142)
0000693C	00004EF0			6046+	DC	A(T143)
00006940	00004F60			6047+	DC	A(T144)
00006944	00004FD0			6048+	DC	A(T145)
00006948	00005040			6049+	DC	A(T146)
0000694C	000050B0			6050+	DC	A(T147)
00006950	00005120			6051+	DC	A(T148)
00006954	00005190			6052+	DC	A(T149)
00006958	00005200			6053+	DC	A(T150)
0000695C	00005270			6054+	DC	A(T151)
00006960	000052E0			6055+	DC	A(T152)
00006964	00005350			6056+	DC	A(T153)
00006968	000053C0			6057+	DC	A(T154)
0000696C	00005430			6058+	DC	A(T155)
00006970	000054A0			6059+	DC	A(T156)
00006974	00005510			6060+	DC	A(T157)
00006978	00005580			6061+	DC	A(T158)
0000697C	000055F0			6062+	DC	A(T159)
00006980	00005660			6063+	DC	A(T160)
00006984	000056D0			6064+	DC	A(T161)
00006988	00005740			6065+	DC	A(T162)



LOC	OBJECT CODE	ADDR1	ADDR2	STMT	
				6108	*****
				6109	*            Register equates
				6110	*****
		00000000	00000001	6112 R0	EQU 0
		00000001	00000001	6113 R1	EQU 1
		00000002	00000001	6114 R2	EQU 2
		00000003	00000001	6115 R3	EQU 3
		00000004	00000001	6116 R4	EQU 4
		00000005	00000001	6117 R5	EQU 5
		00000006	00000001	6118 R6	EQU 6
		00000007	00000001	6119 R7	EQU 7
		00000008	00000001	6120 R8	EQU 8
		00000009	00000001	6121 R9	EQU 9
		0000000A	00000001	6122 R10	EQU 10
		0000000B	00000001	6123 R11	EQU 11
		0000000C	00000001	6124 R12	EQU 12
		0000000D	00000001	6125 R13	EQU 13
		0000000E	00000001	6126 R14	EQU 14
		0000000F	00000001	6127 R15	EQU 15
				6129	*****
				6130	*            Register equates
				6131	*****
		00000000	00000001	6133 V0	EQU 0
		00000001	00000001	6134 V1	EQU 1
		00000002	00000001	6135 V2	EQU 2
		00000003	00000001	6136 V3	EQU 3
		00000004	00000001	6137 V4	EQU 4
		00000005	00000001	6138 V5	EQU 5
		00000006	00000001	6139 V6	EQU 6
		00000007	00000001	6140 V7	EQU 7
		00000008	00000001	6141 V8	EQU 8
		00000009	00000001	6142 V9	EQU 9
		0000000A	00000001	6143 V10	EQU 10
		0000000B	00000001	6144 V11	EQU 11
		0000000C	00000001	6145 V12	EQU 12
		0000000D	00000001	6146 V13	EQU 13
		0000000E	00000001	6147 V14	EQU 14
		0000000F	00000001	6148 V15	EQU 15
		00000010	00000001	6149 V16	EQU 16
		00000011	00000001	6150 V17	EQU 17
		00000012	00000001	6151 V18	EQU 18
		00000013	00000001	6152 V19	EQU 19
		00000014	00000001	6153 V20	EQU 20
		00000015	00000001	6154 V21	EQU 21





SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES														
BEGIN	I	00000200	2	151	117	147	148	149											
CTLR0	F	000004BC	4	360	161	162	163	164											
DECNUM	C	0000108B	16	415	260	262	269	271	276	278	283	285							
E7TEST	4	00000000	72	429	210														
E7TESTS	F	00006704	4	5901	203														
EDIT	X	0000105F	18	410	261	270	277	284											
ENDTEST	U	00000318	1	246	208														
E0J	I	000004A0	4	350	196	249													
E0JPSW	D	00000490	8	348	350														
FAILCONT	U	00000308	1	236															
FAILED	F	00001000	4	388	238	247													
FAILMSG	U	00000304	1	230	220														
FAILPSW	D	000004A8	8	352	354														
FAILTEST	I	000004B8	4	354	250														
FB0001	F	00000280	8	180	184	185	187												
I2	U	00000008	1	435	268														
I3	U	00000009	1	436	275														
IMAGE	1	00000000	27176	0															
K	U	00000400	1	372	373	374	375												
K64	U	00010000	1	374															
M	U	00000007	1	434	282														
MB	U	00100000	1	375															
MSG	I	000003D8	4	310	195	293													
MSGCMD	C	00000426	9	340	323	324													
MSGMSG	C	0000042F	95	341	317	338	315												
MSGMVC	I	00000420	6	338	321														
MSGOK	I	000003EE	2	319	316														
MSGRET	I	0000040E	4	334	327	330													
MSGSAVE	F	00000414	4	337	313	334													
NEXTE7	U	000002D4	1	205	223	241													
OPNAME	C	0000000A	8	438	265														
PAGE	U	00001000	1	373															
PRT3	C	00001075	18	413	261	262	263	270	271	272	277	278	279	284	285	286			
PRTI2	C	00001044	2	399	272														
PRTI3	C	00001050	2	401	279														
PRTLNE	C	00001008	16	394	405	292													
PRTLNG	U	00000057	1	405	291														
PRTM	C	0000105C	2	403	286														
PRTNAME	C	00001033	8	397	265														
PRTNUM	C	00001018	3	395	263														
R0	U	00000000	1	6112	111	161	164	184	186	187	188	193	212	213	237	238	290		
					291	294	310	313	315	317	319	334							
R1	U	00000001	1	6113	194	218	219	247	248	292	324	338							
R10	U	0000000A	1	6122	149	158	159												
R11	U	0000000B	1	6123	215	216	562	589	616	643	670	697	727	754	781	808	835		
					865	892	919	946	973	1003	1030	1057	1084	1112	1141	1168	1195		
					1222	1249	1276	1303	1330	1357	1384	1411	1438	1467	1494	1521	1548		
					1575	1602	1629	1656	1683	1710	1737	1766	1793	1820	1847	1874	1901		
					1928	1955	1982	2009	2038	2065	2092	2119	2146	2173	2200	2227	2254		
					2281	2308	2337	2364	2391	2418	2445	2472	2499	2526	2553	2580	2607		
					2634	2661	2688	2715	2742	2769	2796	2825	2852	2879	2906	2933	2960		
					2987	3014	3041	3068	3095	3122	3149	3176	3203	3232	3259	3286	3313		
					3340	3367	3394	3421	3448	3475	3502	3529	3556	3583	3610	3639	3666		
					3693	3720	3747	3774	3801	3828	3855	3882	3909	3936	3963	3990	4019		
					4046	4073	4100	4127	4154	4181	4208	4235	4262	4289	4316	4343	4370		
					4397	4424	4451	4478	4507	4534	4561	4588	4615	4642	4669	4696	4723		



SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
RE107	F	00003F8C	4	3449	3436 3437 3439
RE108	F	00003FFC	4	3476	3463 3464 3466
RE109	F	0000406C	4	3503	3490 3491 3493
RE11	F	0000158C	4	836	823 824 826
RE110	F	000040DC	4	3530	3517 3518 3520
RE111	F	0000414C	4	3557	3544 3545 3547
RE112	F	000041BC	4	3584	3571 3572 3574
RE113	F	0000422C	4	3611	3598 3599 3601
RE114	F	0000429C	4	3640	3627 3628 3630
RE115	F	0000430C	4	3667	3654 3655 3657
RE116	F	0000437C	4	3694	3681 3682 3684
RE117	F	000043EC	4	3721	3708 3709 3711
RE118	F	0000445C	4	3748	3735 3736 3738
RE119	F	000044CC	4	3775	3762 3763 3765
RE12	F	000015FC	4	866	853 854 856
RE120	F	0000453C	4	3802	3789 3790 3792
RE121	F	000045AC	4	3829	3816 3817 3819
RE122	F	0000461C	4	3856	3843 3844 3846
RE123	F	0000468C	4	3883	3870 3871 3873
RE124	F	000046FC	4	3910	3897 3898 3900
RE125	F	0000476C	4	3937	3924 3925 3927
RE126	F	000047DC	4	3964	3951 3952 3954
RE127	F	0000484C	4	3991	3978 3979 3981
RE128	F	000048BC	4	4020	4007 4008 4010
RE129	F	0000492C	4	4047	4034 4035 4037
RE13	F	0000166C	4	893	880 881 883
RE130	F	0000499C	4	4074	4061 4062 4064
RE131	F	00004A0C	4	4101	4088 4089 4091
RE132	F	00004A7C	4	4128	4115 4116 4118
RE133	F	00004AEC	4	4155	4142 4143 4145
RE134	F	00004B5C	4	4182	4169 4170 4172
RE135	F	00004BCC	4	4209	4196 4197 4199
RE136	F	00004C3C	4	4236	4223 4224 4226
RE137	F	00004CAC	4	4263	4250 4251 4253
RE138	F	00004D1C	4	4290	4277 4278 4280
RE139	F	00004D8C	4	4317	4304 4305 4307
RE14	F	000016DC	4	920	907 908 910
RE140	F	00004DFC	4	4344	4331 4332 4334
RE141	F	00004E6C	4	4371	4358 4359 4361
RE142	F	00004EDC	4	4398	4385 4386 4388
RE143	F	00004F4C	4	4425	4412 4413 4415
RE144	F	00004FBC	4	4452	4439 4440 4442
RE145	F	0000502C	4	4479	4466 4467 4469
RE146	F	0000509C	4	4508	4495 4496 4498
RE147	F	0000510C	4	4535	4522 4523 4525
RE148	F	0000517C	4	4562	4549 4550 4552
RE149	F	000051EC	4	4589	4576 4577 4579
RE15	F	0000174C	4	947	934 935 937
RE150	F	0000525C	4	4616	4603 4604 4606
RE151	F	000052CC	4	4643	4630 4631 4633
RE152	F	0000533C	4	4670	4657 4658 4660
RE153	F	000053AC	4	4697	4684 4685 4687
RE154	F	0000541C	4	4724	4711 4712 4714
RE155	F	0000548C	4	4751	4738 4739 4741
RE156	F	000054FC	4	4778	4765 4766 4768
RE157	F	0000556C	4	4805	4792 4793 4795

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
RE158	F	000055DC	4	4832	4819 4820 4822
RE159	F	0000564C	4	4859	4846 4847 4849
RE16	F	000017BC	4	974	961 962 964
RE160	F	000056BC	4	4886	4873 4874 4876
RE161	F	0000572C	4	4913	4900 4901 4903
RE162	F	0000579C	4	4940	4927 4928 4930
RE163	F	0000580C	4	4969	4956 4957 4959
RE164	F	0000587C	4	4996	4983 4984 4986
RE165	F	000058EC	4	5023	5010 5011 5013
RE166	F	0000595C	4	5050	5037 5038 5040
RE167	F	000059CC	4	5077	5064 5065 5067
RE168	F	00005A3C	4	5104	5091 5092 5094
RE169	F	00005AAC	4	5131	5118 5119 5121
RE17	F	0000182C	4	1004	991 992 994
RE170	F	00005B1C	4	5158	5145 5146 5148
RE171	F	00005B8C	4	5185	5172 5173 5175
RE172	F	00005BFC	4	5212	5199 5200 5202
RE173	F	00005C6C	4	5239	5226 5227 5229
RE174	F	00005CDC	4	5266	5253 5254 5256
RE175	F	00005D4C	4	5293	5280 5281 5283
RE176	F	00005DBC	4	5320	5307 5308 5310
RE177	F	00005E2C	4	5347	5334 5335 5337
RE178	F	00005E9C	4	5374	5361 5362 5364
RE179	F	00005F0C	4	5401	5388 5389 5391
RE18	F	0000189C	4	1031	1018 1019 1021
RE180	F	00005F7C	4	5428	5415 5416 5418
RE181	F	00005FEC	4	5457	5444 5445 5447
RE182	F	0000605C	4	5484	5471 5472 5474
RE183	F	000060CC	4	5511	5498 5499 5501
RE184	F	0000613C	4	5538	5525 5526 5528
RE185	F	000061AC	4	5565	5552 5553 5555
RE186	F	0000621C	4	5592	5579 5580 5582
RE187	F	0000628C	4	5619	5606 5607 5609
RE188	F	000062FC	4	5646	5633 5634 5636
RE189	F	0000636C	4	5673	5660 5661 5663
RE19	F	0000190C	4	1058	1045 1046 1048
RE190	F	000063DC	4	5700	5687 5688 5690
RE191	F	0000644C	4	5727	5714 5715 5717
RE192	F	000064BC	4	5754	5741 5742 5744
RE193	F	0000652C	4	5781	5768 5769 5771
RE194	F	0000659C	4	5808	5795 5796 5798
RE195	F	0000660C	4	5835	5822 5823 5825
RE196	F	0000667C	4	5862	5849 5850 5852
RE197	F	000066EC	4	5889	5876 5877 5879
RE2	F	0000119C	4	590	577 578 580
RE20	F	0000197C	4	1085	1072 1073 1075
RE21	F	000019EC	4	1113	1100 1101 1103
RE22	F	00001A5C	4	1142	1129 1130 1132
RE23	F	00001ACC	4	1169	1156 1157 1159
RE24	F	00001B3C	4	1196	1183 1184 1186
RE25	F	00001BAC	4	1223	1210 1211 1213
RE26	F	00001C1C	4	1250	1237 1238 1240
RE27	F	00001C8C	4	1277	1264 1265 1267
RE28	F	00001CFC	4	1304	1291 1292 1294
RE29	F	00001D6C	4	1331	1318 1319 1321
RE3	F	0000120C	4	617	604 605 607



SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
RE30	F	00001DDC	4	1358	1345 1346 1348
RE31	F	00001E4C	4	1385	1372 1373 1375
RE32	F	00001EBC	4	1412	1399 1400 1402
RE33	F	00001F2C	4	1439	1426 1427 1429
RE34	F	00001F9C	4	1468	1455 1456 1458
RE35	F	0000200C	4	1495	1482 1483 1485
RE36	F	0000207C	4	1522	1509 1510 1512
RE37	F	000020EC	4	1549	1536 1537 1539
RE38	F	0000215C	4	1576	1563 1564 1566
RE39	F	000021CC	4	1603	1590 1591 1593
RE4	F	0000127C	4	644	631 632 634
RE40	F	0000223C	4	1630	1617 1618 1620
RE41	F	000022AC	4	1657	1644 1645 1647
RE42	F	0000231C	4	1684	1671 1672 1674
RE43	F	0000238C	4	1711	1698 1699 1701
RE44	F	000023FC	4	1738	1725 1726 1728
RE45	F	0000246C	4	1767	1754 1755 1757
RE46	F	000024DC	4	1794	1781 1782 1784
RE47	F	0000254C	4	1821	1808 1809 1811
RE48	F	000025BC	4	1848	1835 1836 1838
RE49	F	0000262C	4	1875	1862 1863 1865
RE5	F	000012EC	4	671	658 659 661
RE50	F	0000269C	4	1902	1889 1890 1892
RE51	F	0000270C	4	1929	1916 1917 1919
RE52	F	0000277C	4	1956	1943 1944 1946
RE53	F	000027EC	4	1983	1970 1971 1973
RE54	F	0000285C	4	2010	1997 1998 2000
RE55	F	000028CC	4	2039	2026 2027 2029
RE56	F	0000293C	4	2066	2053 2054 2056
RE57	F	000029AC	4	2093	2080 2081 2083
RE58	F	00002A1C	4	2120	2107 2108 2110
RE59	F	00002A8C	4	2147	2134 2135 2137
RE6	F	0000135C	4	698	685 686 688
RE60	F	00002AFC	4	2174	2161 2162 2164
RE61	F	00002B6C	4	2201	2188 2189 2191
RE62	F	00002BDC	4	2228	2215 2216 2218
RE63	F	00002C4C	4	2255	2242 2243 2245
RE64	F	00002CBC	4	2282	2269 2270 2272
RE65	F	00002D2C	4	2309	2296 2297 2299
RE66	F	00002D9C	4	2338	2325 2326 2328
RE67	F	00002E0C	4	2365	2352 2353 2355
RE68	F	00002E7C	4	2392	2379 2380 2382
RE69	F	00002EEC	4	2419	2406 2407 2409
RE7	F	000013CC	4	728	715 716 718
RE70	F	00002F5C	4	2446	2433 2434 2436
RE71	F	00002FCC	4	2473	2460 2461 2463
RE72	F	0000303C	4	2500	2487 2488 2490
RE73	F	000030AC	4	2527	2514 2515 2517
RE74	F	0000311C	4	2554	2541 2542 2544
RE75	F	0000318C	4	2581	2568 2569 2571
RE76	F	000031FC	4	2608	2595 2596 2598
RE77	F	0000326C	4	2635	2622 2623 2625
RE78	F	000032DC	4	2662	2649 2650 2652
RE79	F	0000334C	4	2689	2676 2677 2679
RE8	F	0000143C	4	755	742 743 745
RE80	F	000033BC	4	2716	2703 2704 2706



SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
RE81	F	0000342C	4	2743	2730 2731 2733
RE82	F	0000349C	4	2770	2757 2758 2760
RE83	F	0000350C	4	2797	2784 2785 2787
RE84	F	0000357C	4	2826	2813 2814 2816
RE85	F	000035EC	4	2853	2840 2841 2843
RE86	F	0000365C	4	2880	2867 2868 2870
RE87	F	000036CC	4	2907	2894 2895 2897
RE88	F	0000373C	4	2934	2921 2922 2924
RE89	F	000037AC	4	2961	2948 2949 2951
RE9	F	000014AC	4	782	769 770 772
RE90	F	0000381C	4	2988	2975 2976 2978
RE91	F	0000388C	4	3015	3002 3003 3005
RE92	F	000038FC	4	3042	3029 3030 3032
RE93	F	0000396C	4	3069	3056 3057 3059
RE94	F	000039DC	4	3096	3083 3084 3086
RE95	F	00003A4C	4	3123	3110 3111 3113
RE96	F	00003ABC	4	3150	3137 3138 3140
RE97	F	00003B2C	4	3177	3164 3165 3167
RE98	F	00003B9C	4	3204	3191 3192 3194
RE99	F	00003C0C	4	3233	3220 3221 3223
REA1	A	000010F0	4	553	
REA10	A	000014E0	4	799	
REA100	A	00003C40	4	3250	
REA101	A	00003CB0	4	3277	
REA102	A	00003D20	4	3304	
REA103	A	00003D90	4	3331	
REA104	A	00003E00	4	3358	
REA105	A	00003E70	4	3385	
REA106	A	00003EE0	4	3412	
REA107	A	00003F50	4	3439	
REA108	A	00003FC0	4	3466	
REA109	A	00004030	4	3493	
REA11	A	00001550	4	826	
REA110	A	000040A0	4	3520	
REA111	A	00004110	4	3547	
REA112	A	00004180	4	3574	
REA113	A	000041F0	4	3601	
REA114	A	00004260	4	3630	
REA115	A	000042D0	4	3657	
REA116	A	00004340	4	3684	
REA117	A	000043B0	4	3711	
REA118	A	00004420	4	3738	
REA119	A	00004490	4	3765	
REA12	A	000015C0	4	856	
REA120	A	00004500	4	3792	
REA121	A	00004570	4	3819	
REA122	A	000045E0	4	3846	
REA123	A	00004650	4	3873	
REA124	A	000046C0	4	3900	
REA125	A	00004730	4	3927	
REA126	A	000047A0	4	3954	
REA127	A	00004810	4	3981	
REA128	A	00004880	4	4010	
REA129	A	000048F0	4	4037	
REA13	A	00001630	4	883	
REA130	A	00004960	4	4064	

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
REA131	A	000049D0	4	4091	
REA132	A	00004A40	4	4118	
REA133	A	00004AB0	4	4145	
REA134	A	00004B20	4	4172	
REA135	A	00004B90	4	4199	
REA136	A	00004C00	4	4226	
REA137	A	00004C70	4	4253	
REA138	A	00004CE0	4	4280	
REA139	A	00004D50	4	4307	
REA14	A	000016A0	4	910	
REA140	A	00004DC0	4	4334	
REA141	A	00004E30	4	4361	
REA142	A	00004EA0	4	4388	
REA143	A	00004F10	4	4415	
REA144	A	00004F80	4	4442	
REA145	A	00004FF0	4	4469	
REA146	A	00005060	4	4498	
REA147	A	000050D0	4	4525	
REA148	A	00005140	4	4552	
REA149	A	000051B0	4	4579	
REA15	A	00001710	4	937	
REA150	A	00005220	4	4606	
REA151	A	00005290	4	4633	
REA152	A	00005300	4	4660	
REA153	A	00005370	4	4687	
REA154	A	000053E0	4	4714	
REA155	A	00005450	4	4741	
REA156	A	000054C0	4	4768	
REA157	A	00005530	4	4795	
REA158	A	000055A0	4	4822	
REA159	A	00005610	4	4849	
REA16	A	00001780	4	964	
REA160	A	00005680	4	4876	
REA161	A	000056F0	4	4903	
REA162	A	00005760	4	4930	
REA163	A	000057D0	4	4959	
REA164	A	00005840	4	4986	
REA165	A	000058B0	4	5013	
REA166	A	00005920	4	5040	
REA167	A	00005990	4	5067	
REA168	A	00005A00	4	5094	
REA169	A	00005A70	4	5121	
REA17	A	000017F0	4	994	
REA170	A	00005AE0	4	5148	
REA171	A	00005B50	4	5175	
REA172	A	00005BC0	4	5202	
REA173	A	00005C30	4	5229	
REA174	A	00005CA0	4	5256	
REA175	A	00005D10	4	5283	
REA176	A	00005D80	4	5310	
REA177	A	00005DF0	4	5337	
REA178	A	00005E60	4	5364	
REA179	A	00005ED0	4	5391	
REA18	A	00001860	4	1021	
REA180	A	00005F40	4	5418	
REA181	A	00005FB0	4	5447	

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
REA182	A	00006020	4	5474	
REA183	A	00006090	4	5501	
REA184	A	00006100	4	5528	
REA185	A	00006170	4	5555	
REA186	A	000061E0	4	5582	
REA187	A	00006250	4	5609	
REA188	A	000062C0	4	5636	
REA189	A	00006330	4	5663	
REA19	A	000018D0	4	1048	
REA190	A	000063A0	4	5690	
REA191	A	00006410	4	5717	
REA192	A	00006480	4	5744	
REA193	A	000064F0	4	5771	
REA194	A	00006560	4	5798	
REA195	A	000065D0	4	5825	
REA196	A	00006640	4	5852	
REA197	A	000066B0	4	5879	
REA2	A	00001160	4	580	
REA20	A	00001940	4	1075	
REA21	A	000019B0	4	1103	
REA22	A	00001A20	4	1132	
REA23	A	00001A90	4	1159	
REA24	A	00001B00	4	1186	
REA25	A	00001B70	4	1213	
REA26	A	00001BE0	4	1240	
REA27	A	00001C50	4	1267	
REA28	A	00001CC0	4	1294	
REA29	A	00001D30	4	1321	
REA3	A	000011D0	4	607	
REA30	A	00001DA0	4	1348	
REA31	A	00001E10	4	1375	
REA32	A	00001E80	4	1402	
REA33	A	00001EF0	4	1429	
REA34	A	00001F60	4	1458	
REA35	A	00001FD0	4	1485	
REA36	A	00002040	4	1512	
REA37	A	000020B0	4	1539	
REA38	A	00002120	4	1566	
REA39	A	00002190	4	1593	
REA4	A	00001240	4	634	
REA40	A	00002200	4	1620	
REA41	A	00002270	4	1647	
REA42	A	000022E0	4	1674	
REA43	A	00002350	4	1701	
REA44	A	000023C0	4	1728	
REA45	A	00002430	4	1757	
REA46	A	000024A0	4	1784	
REA47	A	00002510	4	1811	
REA48	A	00002580	4	1838	
REA49	A	000025F0	4	1865	
REA5	A	000012B0	4	661	
REA50	A	00002660	4	1892	
REA51	A	000026D0	4	1919	
REA52	A	00002740	4	1946	
REA53	A	000027B0	4	1973	
REA54	A	00002820	4	2000	

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES	
REA55	A	00002890	4	2029		
REA56	A	00002900	4	2056		
REA57	A	00002970	4	2083		
REA58	A	000029E0	4	2110		
REA59	A	00002A50	4	2137		
REA6	A	00001320	4	688		
REA60	A	00002AC0	4	2164		
REA61	A	00002B30	4	2191		
REA62	A	00002BA0	4	2218		
REA63	A	00002C10	4	2245		
REA64	A	00002C80	4	2272		
REA65	A	00002CF0	4	2299		
REA66	A	00002D60	4	2328		
REA67	A	00002DD0	4	2355		
REA68	A	00002E40	4	2382		
REA69	A	00002EB0	4	2409		
REA7	A	00001390	4	718		
REA70	A	00002F20	4	2436		
REA71	A	00002F90	4	2463		
REA72	A	00003000	4	2490		
REA73	A	00003070	4	2517		
REA74	A	000030E0	4	2544		
REA75	A	00003150	4	2571		
REA76	A	000031C0	4	2598		
REA77	A	00003230	4	2625		
REA78	A	000032A0	4	2652		
REA79	A	00003310	4	2679		
REA8	A	00001400	4	745		
REA80	A	00003380	4	2706		
REA81	A	000033F0	4	2733		
REA82	A	00003460	4	2760		
REA83	A	000034D0	4	2787		
REA84	A	00003540	4	2816		
REA85	A	000035B0	4	2843		
REA86	A	00003620	4	2870		
REA87	A	00003690	4	2897		
REA88	A	00003700	4	2924		
REA89	A	00003770	4	2951		
REA9	A	00001470	4	772		
REA90	A	000037E0	4	2978		
REA91	A	00003850	4	3005		
REA92	A	000038C0	4	3032		
REA93	A	00003930	4	3059		
REA94	A	000039A0	4	3086		
REA95	A	00003A10	4	3113		
REA96	A	00003A80	4	3140		
REA97	A	00003AF0	4	3167		
REA98	A	00003B60	4	3194		
REA99	A	00003BD0	4	3223		
READDR	A	00000020	4	442	218	
REG2LOW	U	000000DD	1	378		
REG2PATT	U	AABBCCDD	1	377		
RELEN	A	0000001C	4	441		
RPTDWSAV	D	000003C8	8	303	290	294
RPTERROR	I	00000326	4	256	231	
RPTSAVE	F	000003C0	4	300	256	297

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
RPTSVR5	F	000003C4	4	301	257 296
SKL0001	U	0000004E	1	177	193
SKT0001	C	0000022A	20	174	177 194
SVOLDPSW	U	00000140	0	113	
T1	A	000010D0	4	543	5904
T10	A	000014C0	4	789	5913
T100	A	00003C20	4	3240	6003
T101	A	00003C90	4	3267	6004
T102	A	00003D00	4	3294	6005
T103	A	00003D70	4	3321	6006
T104	A	00003DE0	4	3348	6007
T105	A	00003E50	4	3375	6008
T106	A	00003EC0	4	3402	6009
T107	A	00003F30	4	3429	6010
T108	A	00003FA0	4	3456	6011
T109	A	00004010	4	3483	6012
T11	A	00001530	4	816	5914
T110	A	00004080	4	3510	6013
T111	A	000040F0	4	3537	6014
T112	A	00004160	4	3564	6015
T113	A	000041D0	4	3591	6016
T114	A	00004240	4	3620	6017
T115	A	000042B0	4	3647	6018
T116	A	00004320	4	3674	6019
T117	A	00004390	4	3701	6020
T118	A	00004400	4	3728	6021
T119	A	00004470	4	3755	6022
T12	A	000015A0	4	846	5915
T120	A	000044E0	4	3782	6023
T121	A	00004550	4	3809	6024
T122	A	000045C0	4	3836	6025
T123	A	00004630	4	3863	6026
T124	A	000046A0	4	3890	6027
T125	A	00004710	4	3917	6028
T126	A	00004780	4	3944	6029
T127	A	000047F0	4	3971	6030
T128	A	00004860	4	4000	6031
T129	A	000048D0	4	4027	6032
T13	A	00001610	4	873	5916
T130	A	00004940	4	4054	6033
T131	A	000049B0	4	4081	6034
T132	A	00004A20	4	4108	6035
T133	A	00004A90	4	4135	6036
T134	A	00004B00	4	4162	6037
T135	A	00004B70	4	4189	6038
T136	A	00004BE0	4	4216	6039
T137	A	00004C50	4	4243	6040
T138	A	00004CC0	4	4270	6041
T139	A	00004D30	4	4297	6042
T14	A	00001680	4	900	5917
T140	A	00004DA0	4	4324	6043
T141	A	00004E10	4	4351	6044
T142	A	00004E80	4	4378	6045
T143	A	00004EF0	4	4405	6046
T144	A	00004F60	4	4432	6047
T145	A	00004FD0	4	4459	6048



SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
T146	A	00005040	4	4488	6049
T147	A	000050B0	4	4515	6050
T148	A	00005120	4	4542	6051
T149	A	00005190	4	4569	6052
T15	A	000016F0	4	927	5918
T150	A	00005200	4	4596	6053
T151	A	00005270	4	4623	6054
T152	A	000052E0	4	4650	6055
T153	A	00005350	4	4677	6056
T154	A	000053C0	4	4704	6057
T155	A	00005430	4	4731	6058
T156	A	000054A0	4	4758	6059
T157	A	00005510	4	4785	6060
T158	A	00005580	4	4812	6061
T159	A	000055F0	4	4839	6062
T16	A	00001760	4	954	5919
T160	A	00005660	4	4866	6063
T161	A	000056D0	4	4893	6064
T162	A	00005740	4	4920	6065
T163	A	000057B0	4	4949	6066
T164	A	00005820	4	4976	6067
T165	A	00005890	4	5003	6068
T166	A	00005900	4	5030	6069
T167	A	00005970	4	5057	6070
T168	A	000059E0	4	5084	6071
T169	A	00005A50	4	5111	6072
T17	A	000017D0	4	984	5920
T170	A	00005AC0	4	5138	6073
T171	A	00005B30	4	5165	6074
T172	A	00005BA0	4	5192	6075
T173	A	00005C10	4	5219	6076
T174	A	00005C80	4	5246	6077
T175	A	00005CF0	4	5273	6078
T176	A	00005D60	4	5300	6079
T177	A	00005DD0	4	5327	6080
T178	A	00005E40	4	5354	6081
T179	A	00005EB0	4	5381	6082
T18	A	00001840	4	1011	5921
T180	A	00005F20	4	5408	6083
T181	A	00005F90	4	5437	6084
T182	A	00006000	4	5464	6085
T183	A	00006070	4	5491	6086
T184	A	000060E0	4	5518	6087
T185	A	00006150	4	5545	6088
T186	A	000061C0	4	5572	6089
T187	A	00006230	4	5599	6090
T188	A	000062A0	4	5626	6091
T189	A	00006310	4	5653	6092
T19	A	000018B0	4	1038	5922
T190	A	00006380	4	5680	6093
T191	A	000063F0	4	5707	6094
T192	A	00006460	4	5734	6095
T193	A	000064D0	4	5761	6096
T194	A	00006540	4	5788	6097
T195	A	000065B0	4	5815	6098
T196	A	00006620	4	5842	6099

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
T197	A	00006690	4	5869	6100
T2	A	00001140	4	570	5905
T20	A	00001920	4	1065	5923
T21	A	00001990	4	1093	5924
T22	A	00001A00	4	1122	5925
T23	A	00001A70	4	1149	5926
T24	A	00001AE0	4	1176	5927
T25	A	00001B50	4	1203	5928
T26	A	00001BC0	4	1230	5929
T27	A	00001C30	4	1257	5930
T28	A	00001CA0	4	1284	5931
T29	A	00001D10	4	1311	5932
T3	A	000011B0	4	597	5906
T30	A	00001D80	4	1338	5933
T31	A	00001DF0	4	1365	5934
T32	A	00001E60	4	1392	5935
T33	A	00001ED0	4	1419	5936
T34	A	00001F40	4	1448	5937
T35	A	00001FB0	4	1475	5938
T36	A	00002020	4	1502	5939
T37	A	00002090	4	1529	5940
T38	A	00002100	4	1556	5941
T39	A	00002170	4	1583	5942
T4	A	00001220	4	624	5907
T40	A	000021E0	4	1610	5943
T41	A	00002250	4	1637	5944
T42	A	000022C0	4	1664	5945
T43	A	00002330	4	1691	5946
T44	A	000023A0	4	1718	5947
T45	A	00002410	4	1747	5948
T46	A	00002480	4	1774	5949
T47	A	000024F0	4	1801	5950
T48	A	00002560	4	1828	5951
T49	A	000025D0	4	1855	5952
T5	A	00001290	4	651	5908
T50	A	00002640	4	1882	5953
T51	A	000026B0	4	1909	5954
T52	A	00002720	4	1936	5955
T53	A	00002790	4	1963	5956
T54	A	00002800	4	1990	5957
T55	A	00002870	4	2019	5958
T56	A	000028E0	4	2046	5959
T57	A	00002950	4	2073	5960
T58	A	000029C0	4	2100	5961
T59	A	00002A30	4	2127	5962
T6	A	00001300	4	678	5909
T60	A	00002AA0	4	2154	5963
T61	A	00002B10	4	2181	5964
T62	A	00002B80	4	2208	5965
T63	A	00002BF0	4	2235	5966
T64	A	00002C60	4	2262	5967
T65	A	00002CD0	4	2289	5968
T66	A	00002D40	4	2318	5969
T67	A	00002DB0	4	2345	5970
T68	A	00002E20	4	2372	5971
T69	A	00002E90	4	2399	5972

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES													
T7	A	00001370	4	708	5910													
T70	A	00002F00	4	2426	5973													
T71	A	00002F70	4	2453	5974													
T72	A	00002FE0	4	2480	5975													
T73	A	00003050	4	2507	5976													
T74	A	000030C0	4	2534	5977													
T75	A	00003130	4	2561	5978													
T76	A	000031A0	4	2588	5979													
T77	A	00003210	4	2615	5980													
T78	A	00003280	4	2642	5981													
T79	A	000032F0	4	2669	5982													
T8	A	000013E0	4	735	5911													
T80	A	00003360	4	2696	5983													
T81	A	000033D0	4	2723	5984													
T82	A	00003440	4	2750	5985													
T83	A	000034B0	4	2777	5986													
T84	A	00003520	4	2806	5987													
T85	A	00003590	4	2833	5988													
T86	A	00003600	4	2860	5989													
T87	A	00003670	4	2887	5990													
T88	A	000036E0	4	2914	5991													
T89	A	00003750	4	2941	5992													
T9	A	00001450	4	762	5912													
T90	A	000037C0	4	2968	5993													
T91	A	00003830	4	2995	5994													
T92	A	000038A0	4	3022	5995													
T93	A	00003910	4	3049	5996													
T94	A	00003980	4	3076	5997													
T95	A	000039F0	4	3103	5998													
T96	A	00003A60	4	3130	5999													
T97	A	00003AD0	4	3157	6000													
T98	A	00003B40	4	3184	6001													
T99	A	00003BB0	4	3213	6002													
TESTING	F	00001004	4	389	213													
TNUM	H	00000004	2	431	212	259												
TSUB	A	00000000	4	430	215													
TTABLE	F	00006704	4	5903														
V0	U	00000000	1	6133														
V1	U	00000001	1	6134														
V10	U	0000000A	1	6143														
V11	U	0000000B	1	6144														
V12	U	0000000C	1	6145														
V13	U	0000000D	1	6146														
V14	U	0000000E	1	6147														
V15	U	0000000F	1	6148														
V16	U	00000010	1	6149														
V17	U	00000011	1	6150														
V18	U	00000012	1	6151														
V19	U	00000013	1	6152														
V1FUDGE	X	000010AC	16	422	559	586	613	640	667	694	724	751	778	805	832	862	889	
					916	943	970	1000	1027	1054	1081	1109	1138	1165	1192	1219	1246	
					1273	1300	1327	1354	1381	1408	1435	1464	1491	1518	1545	1572	1599	
					1626	1653	1680	1707	1734	1763	1790	1817	1844	1871	1898	1925	1952	
					1979	2006	2035	2062	2089	2116	2143	2170	2197	2224	2251	2278	2305	
					2334	2361	2388	2415	2442	2469	2496	2523	2550	2577	2604	2631	2658	
					2685	2712	2739	2766	2793	2822	2849	2876	2903	2930	2957	2984	3011	



SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
V10141	X	00004E40	16	4363	4369
V10142	X	00004EB0	16	4390	4396
V10143	X	00004F20	16	4417	4423
V10144	X	00004F90	16	4444	4450
V10145	X	00005000	16	4471	4477
V10146	X	00005070	16	4500	4506
V10147	X	000050E0	16	4527	4533
V10148	X	00005150	16	4554	4560
V10149	X	000051C0	16	4581	4587
V1015	X	00001720	16	939	945
V10150	X	00005230	16	4608	4614
V10151	X	000052A0	16	4635	4641
V10152	X	00005310	16	4662	4668
V10153	X	00005380	16	4689	4695
V10154	X	000053F0	16	4716	4722
V10155	X	00005460	16	4743	4749
V10156	X	000054D0	16	4770	4776
V10157	X	00005540	16	4797	4803
V10158	X	000055B0	16	4824	4830
V10159	X	00005620	16	4851	4857
V1016	X	00001790	16	966	972
V10160	X	00005690	16	4878	4884
V10161	X	00005700	16	4905	4911
V10162	X	00005770	16	4932	4938
V10163	X	000057E0	16	4961	4967
V10164	X	00005850	16	4988	4994
V10165	X	000058C0	16	5015	5021
V10166	X	00005930	16	5042	5048
V10167	X	000059A0	16	5069	5075
V10168	X	00005A10	16	5096	5102
V10169	X	00005A80	16	5123	5129
V1017	X	00001800	16	996	1002
V10170	X	00005AF0	16	5150	5156
V10171	X	00005B60	16	5177	5183
V10172	X	00005BD0	16	5204	5210
V10173	X	00005C40	16	5231	5237
V10174	X	00005CB0	16	5258	5264
V10175	X	00005D20	16	5285	5291
V10176	X	00005D90	16	5312	5318
V10177	X	00005E00	16	5339	5345
V10178	X	00005E70	16	5366	5372
V10179	X	00005EE0	16	5393	5399
V1018	X	00001870	16	1023	1029
V10180	X	00005F50	16	5420	5426
V10181	X	00005FC0	16	5449	5455
V10182	X	00006030	16	5476	5482
V10183	X	000060A0	16	5503	5509
V10184	X	00006110	16	5530	5536
V10185	X	00006180	16	5557	5563
V10186	X	000061F0	16	5584	5590
V10187	X	00006260	16	5611	5617
V10188	X	000062D0	16	5638	5644
V10189	X	00006340	16	5665	5671
V1019	X	000018E0	16	1050	1056
V10190	X	000063B0	16	5692	5698
V10191	X	00006420	16	5719	5725



SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
V10192	X	00006490	16	5746	5752
V10193	X	00006500	16	5773	5779
V10194	X	00006570	16	5800	5806
V10195	X	000065E0	16	5827	5833
V10196	X	00006650	16	5854	5860
V10197	X	000066C0	16	5881	5887
V102	X	00001170	16	582	588
V1020	X	00001950	16	1077	1083
V1021	X	000019C0	16	1105	1111
V1022	X	00001A30	16	1134	1140
V1023	X	00001AA0	16	1161	1167
V1024	X	00001B10	16	1188	1194
V1025	X	00001B80	16	1215	1221
V1026	X	00001BF0	16	1242	1248
V1027	X	00001C60	16	1269	1275
V1028	X	00001CD0	16	1296	1302
V1029	X	00001D40	16	1323	1329
V103	X	000011E0	16	609	615
V1030	X	00001DB0	16	1350	1356
V1031	X	00001E20	16	1377	1383
V1032	X	00001E90	16	1404	1410
V1033	X	00001F00	16	1431	1437
V1034	X	00001F70	16	1460	1466
V1035	X	00001FE0	16	1487	1493
V1036	X	00002050	16	1514	1520
V1037	X	000020C0	16	1541	1547
V1038	X	00002130	16	1568	1574
V1039	X	000021A0	16	1595	1601
V104	X	00001250	16	636	642
V1040	X	00002210	16	1622	1628
V1041	X	00002280	16	1649	1655
V1042	X	000022F0	16	1676	1682
V1043	X	00002360	16	1703	1709
V1044	X	000023D0	16	1730	1736
V1045	X	00002440	16	1759	1765
V1046	X	000024B0	16	1786	1792
V1047	X	00002520	16	1813	1819
V1048	X	00002590	16	1840	1846
V1049	X	00002600	16	1867	1873
V105	X	000012C0	16	663	669
V1050	X	00002670	16	1894	1900
V1051	X	000026E0	16	1921	1927
V1052	X	00002750	16	1948	1954
V1053	X	000027C0	16	1975	1981
V1054	X	00002830	16	2002	2008
V1055	X	000028A0	16	2031	2037
V1056	X	00002910	16	2058	2064
V1057	X	00002980	16	2085	2091
V1058	X	000029F0	16	2112	2118
V1059	X	00002A60	16	2139	2145
V106	X	00001330	16	690	696
V1060	X	00002AD0	16	2166	2172
V1061	X	00002B40	16	2193	2199
V1062	X	00002BB0	16	2220	2226
V1063	X	00002C20	16	2247	2253
V1064	X	00002C90	16	2274	2280

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES												
V1065	X	00002D00	16	2301	2307												
V1066	X	00002D70	16	2330	2336												
V1067	X	00002DE0	16	2357	2363												
V1068	X	00002E50	16	2384	2390												
V1069	X	00002EC0	16	2411	2417												
V107	X	000013A0	16	720	726												
V1070	X	00002F30	16	2438	2444												
V1071	X	00002FA0	16	2465	2471												
V1072	X	00003010	16	2492	2498												
V1073	X	00003080	16	2519	2525												
V1074	X	000030F0	16	2546	2552												
V1075	X	00003160	16	2573	2579												
V1076	X	000031D0	16	2600	2606												
V1077	X	00003240	16	2627	2633												
V1078	X	000032B0	16	2654	2660												
V1079	X	00003320	16	2681	2687												
V108	X	00001410	16	747	753												
V1080	X	00003390	16	2708	2714												
V1081	X	00003400	16	2735	2741												
V1082	X	00003470	16	2762	2768												
V1083	X	000034E0	16	2789	2795												
V1084	X	00003550	16	2818	2824												
V1085	X	000035C0	16	2845	2851												
V1086	X	00003630	16	2872	2878												
V1087	X	000036A0	16	2899	2905												
V1088	X	00003710	16	2926	2932												
V1089	X	00003780	16	2953	2959												
V109	X	00001480	16	774	780												
V1090	X	000037F0	16	2980	2986												
V1091	X	00003860	16	3007	3013												
V1092	X	000038D0	16	3034	3040												
V1093	X	00003940	16	3061	3067												
V1094	X	000039B0	16	3088	3094												
V1095	X	00003A20	16	3115	3121												
V1096	X	00003A90	16	3142	3148												
V1097	X	00003B00	16	3169	3175												
V1098	X	00003B70	16	3196	3202												
V1099	X	00003BE0	16	3225	3231												
V10UTPUT	X	00000030	16	444	219												
V2	U	00000002	1	6135													
V20	U	00000014	1	6153													
V21	U	00000015	1	6154													
V22	U	00000016	1	6155	559	560	561	586	587	588	613	614	615	640	641	642	667
					668	669	694	695	696	724	725	726	751	752	753	778	779
					780	805	806	807	832	833	834	862	863	864	889	890	891
					916	917	918	943	944	945	970	971	972	1000	1001	1002	1027
					1028	1029	1054	1055	1056	1081	1082	1083	1109	1110	1111	1138	1139
					1140	1165	1166	1167	1192	1193	1194	1219	1220	1221	1246	1247	1248
					1273	1274	1275	1300	1301	1302	1327	1328	1329	1354	1355	1356	1381
					1382	1383	1408	1409	1410	1435	1436	1437	1464	1465	1466	1491	1492
					1493	1518	1519	1520	1545	1546	1547	1572	1573	1574	1599	1600	1601
					1626	1627	1628	1653	1654	1655	1680	1681	1682	1707	1708	1709	1734
					1735	1736	1763	1764	1765	1790	1791	1792	1817	1818	1819	1844	1845
					1846	1871	1872	1873	1898	1899	1900	1925	1926	1927	1952	1953	1954
					1979	1980	1981	2006	2007	2008	2035	2036	2037	2062	2063	2064	2089
					2090	2091	2116	2117	2118	2143	2144	2145	2170	2171	2172	2197	2198



SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
X103	F	00003DB8	4	3336	3321
X104	F	00003E28	4	3363	3348
X105	F	00003E98	4	3390	3375
X106	F	00003F08	4	3417	3402
X107	F	00003F78	4	3444	3429
X108	F	00003FE8	4	3471	3456
X109	F	00004058	4	3498	3483
X11	F	00001578	4	831	816
X110	F	000040C8	4	3525	3510
X111	F	00004138	4	3552	3537
X112	F	000041A8	4	3579	3564
X113	F	00004218	4	3606	3591
X114	F	00004288	4	3635	3620
X115	F	000042F8	4	3662	3647
X116	F	00004368	4	3689	3674
X117	F	000043D8	4	3716	3701
X118	F	00004448	4	3743	3728
X119	F	000044B8	4	3770	3755
X12	F	000015E8	4	861	846
X120	F	00004528	4	3797	3782
X121	F	00004598	4	3824	3809
X122	F	00004608	4	3851	3836
X123	F	00004678	4	3878	3863
X124	F	000046E8	4	3905	3890
X125	F	00004758	4	3932	3917
X126	F	000047C8	4	3959	3944
X127	F	00004838	4	3986	3971
X128	F	000048A8	4	4015	4000
X129	F	00004918	4	4042	4027
X13	F	00001658	4	888	873
X130	F	00004988	4	4069	4054
X131	F	000049F8	4	4096	4081
X132	F	00004A68	4	4123	4108
X133	F	00004AD8	4	4150	4135
X134	F	00004B48	4	4177	4162
X135	F	00004BB8	4	4204	4189
X136	F	00004C28	4	4231	4216
X137	F	00004C98	4	4258	4243
X138	F	00004D08	4	4285	4270
X139	F	00004D78	4	4312	4297
X14	F	000016C8	4	915	900
X140	F	00004DE8	4	4339	4324
X141	F	00004E58	4	4366	4351
X142	F	00004EC8	4	4393	4378
X143	F	00004F38	4	4420	4405
X144	F	00004FA8	4	4447	4432
X145	F	00005018	4	4474	4459
X146	F	00005088	4	4503	4488
X147	F	000050F8	4	4530	4515
X148	F	00005168	4	4557	4542
X149	F	000051D8	4	4584	4569
X15	F	00001738	4	942	927
X150	F	00005248	4	4611	4596
X151	F	000052B8	4	4638	4623
X152	F	00005328	4	4665	4650
X153	F	00005398	4	4692	4677

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
X154	F	00005408	4	4719	4704
X155	F	00005478	4	4746	4731
X156	F	000054E8	4	4773	4758
X157	F	00005558	4	4800	4785
X158	F	000055C8	4	4827	4812
X159	F	00005638	4	4854	4839
X16	F	000017A8	4	969	954
X160	F	000056A8	4	4881	4866
X161	F	00005718	4	4908	4893
X162	F	00005788	4	4935	4920
X163	F	000057F8	4	4964	4949
X164	F	00005868	4	4991	4976
X165	F	000058D8	4	5018	5003
X166	F	00005948	4	5045	5030
X167	F	000059B8	4	5072	5057
X168	F	00005A28	4	5099	5084
X169	F	00005A98	4	5126	5111
X17	F	00001818	4	999	984
X170	F	00005B08	4	5153	5138
X171	F	00005B78	4	5180	5165
X172	F	00005BE8	4	5207	5192
X173	F	00005C58	4	5234	5219
X174	F	00005CC8	4	5261	5246
X175	F	00005D38	4	5288	5273
X176	F	00005DA8	4	5315	5300
X177	F	00005E18	4	5342	5327
X178	F	00005E88	4	5369	5354
X179	F	00005EF8	4	5396	5381
X18	F	00001888	4	1026	1011
X180	F	00005F68	4	5423	5408
X181	F	00005FD8	4	5452	5437
X182	F	00006048	4	5479	5464
X183	F	000060B8	4	5506	5491
X184	F	00006128	4	5533	5518
X185	F	00006198	4	5560	5545
X186	F	00006208	4	5587	5572
X187	F	00006278	4	5614	5599
X188	F	000062E8	4	5641	5626
X189	F	00006358	4	5668	5653
X19	F	000018F8	4	1053	1038
X190	F	000063C8	4	5695	5680
X191	F	00006438	4	5722	5707
X192	F	000064A8	4	5749	5734
X193	F	00006518	4	5776	5761
X194	F	00006588	4	5803	5788
X195	F	000065F8	4	5830	5815
X196	F	00006668	4	5857	5842
X197	F	000066D8	4	5884	5869
X2	F	00001188	4	585	570
X20	F	00001968	4	1080	1065
X21	F	000019D8	4	1108	1093
X22	F	00001A48	4	1137	1122
X23	F	00001AB8	4	1164	1149
X24	F	00001B28	4	1191	1176
X25	F	00001B98	4	1218	1203
X26	F	00001C08	4	1245	1230



SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
X27	F	00001C78	4	1272	1257
X28	F	00001CE8	4	1299	1284
X29	F	00001D58	4	1326	1311
X3	F	000011F8	4	612	597
X30	F	00001DC8	4	1353	1338
X31	F	00001E38	4	1380	1365
X32	F	00001EA8	4	1407	1392
X33	F	00001F18	4	1434	1419
X34	F	00001F88	4	1463	1448
X35	F	00001FF8	4	1490	1475
X36	F	00002068	4	1517	1502
X37	F	000020D8	4	1544	1529
X38	F	00002148	4	1571	1556
X39	F	000021B8	4	1598	1583
X4	F	00001268	4	639	624
X40	F	00002228	4	1625	1610
X41	F	00002298	4	1652	1637
X42	F	00002308	4	1679	1664
X43	F	00002378	4	1706	1691
X44	F	000023E8	4	1733	1718
X45	F	00002458	4	1762	1747
X46	F	000024C8	4	1789	1774
X47	F	00002538	4	1816	1801
X48	F	000025A8	4	1843	1828
X49	F	00002618	4	1870	1855
X5	F	000012D8	4	666	651
X50	F	00002688	4	1897	1882
X51	F	000026F8	4	1924	1909
X52	F	00002768	4	1951	1936
X53	F	000027D8	4	1978	1963
X54	F	00002848	4	2005	1990
X55	F	000028B8	4	2034	2019
X56	F	00002928	4	2061	2046
X57	F	00002998	4	2088	2073
X58	F	00002A08	4	2115	2100
X59	F	00002A78	4	2142	2127
X6	F	00001348	4	693	678
X60	F	00002AE8	4	2169	2154
X61	F	00002B58	4	2196	2181
X62	F	00002BC8	4	2223	2208
X63	F	00002C38	4	2250	2235
X64	F	00002CA8	4	2277	2262
X65	F	00002D18	4	2304	2289
X66	F	00002D88	4	2333	2318
X67	F	00002DF8	4	2360	2345
X68	F	00002E68	4	2387	2372
X69	F	00002ED8	4	2414	2399
X7	F	000013B8	4	723	708
X70	F	00002F48	4	2441	2426
X71	F	00002FB8	4	2468	2453
X72	F	00003028	4	2495	2480
X73	F	00003098	4	2522	2507
X74	F	00003108	4	2549	2534
X75	F	00003178	4	2576	2561
X76	F	000031E8	4	2603	2588
X77	F	00003258	4	2630	2615





DESC	SYMBOL	SIZE	POS	ADDR
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**Entry: 0**

Image	IMAGE	27176	0000- 6A27	0000- 6A27
Regi on		27176	0000- 6A27	0000- 6A27
CSECT	ZVE7TST	27176	0000- 6A27	0000- 6A27

STMT	FILE NAME
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1 /home/tn529/sharedvfp/tests/zvector-e7-26-VGM asm
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**\*\* NO ERRORS FOUND \*\***